Reg. No. : | | | | | | | | | | |

Question Paper Code: 31042

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2015.

Third Semester

Electronics and Communication Engineering

01UEC302 - DIGITAL ELECTRONICS AND DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Obtain the *XS-3* code and 9's complement for $(428)_{10}$.
2. Find the complement of $A + BC + AB$.
3. Draw the logic diagram of a 4-bit adder- subtractor circuit.
4. What is data selector?
5. Mention the problems faced by ripple counter.
6. If a serial-in-serial-out shift register has n stages and if the clock frequency is f, what will be the time delay between input and output?
7. List the advantages of CMOS logic.
8. Why dynamic RAMs require refreshing?
9. Mention the steps involved in the design using ASM chart.
10. Write a verilog code to perform one's complement.

PART - B (5 x 16 = 80 Marks)

11. (a) (i) Using k-map method, obtain the minimal SOP and POS expressions for the function. $f(x, y, z, w) = \sum m(1, 3, 4, 5, 6, 7, 9, 12, 13)$. (8)

(ii) Simplify the following expression using Boolean laws: (8)

$Y = (A + C)(A + D)(B + C)(B + D)$

$Y = (B + BC)(B + B'C)(B+D)$

Or

(b) (i) Simplify the following function using tabulation method.

$f(A, B, C, D) = \sum m(2, 3, 7, 9, 11, 13) + \sum d(1, 10, 15)$ (10)

(ii) Obtain the three level NOR - NOR implementation of $f(a, b, c, d, e, f) = (ab + cd)ef$. (6)

12. (a) (i) Implement the full subtractor using a 1: 8 demultiplexer. (6)

(ii) Implement the following Boolean function using 16:1 multiplexer $f(A, B, C, D, E) = \sum m(2, 4, 5, 7, 10, 14, 15, 16, 17, 25, 26, 30, 31)$ (10)

Or

(b) (i) Design a BCD to Gray code convertor. Use don't cares. (8)

(ii) Implement 3 x 8 decoder using 2 x 4 decoder. (8)

13. (a) (i) Narrate the operating principle of master slave JK flip flop. (6)

(ii) Design a MOD-6 synchronous counter using J-K Flip-Flops. (10)

Or

(b) (i) Design and draw a 3 bit synchronous counter which goes through the following states: $1 – 3 – 5 – 7 – 1$ (10)

(ii) Show 4 bit data 1010 in series form and parallel form using timing diagram. (6)

14. (a) (i) With the neat sketch comment the operation of 2 input TTL NAND gate with Totem-pole output. (8)

(ii) Narrate the operation of 2 input CMOS NAND and NOR gates. (8)

Or

(b) Design a Two-Bit Magnitude Comparator with a PLA. (16)

15. (a) Narrate the different types of Hazards. Discuss in detail how the hazards can be eliminated. (16)

Or

(b) (i) Illustrate with an example the hierarchical modeling concepts used in Verilog HDL. (10)

(ii) Write a Verilog code to perform 4 bit Full Adder with carry look ahead. (6)