Reg. No. : | | | | | | | | | | |

Question Paper Code: 49271

M.E. DEGREE EXAMINATION, MAY 2015.

Elective

VLSI Design

14PVL504 – PHYSICAL DESIGN OF VLSI CIRCUITS

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (5 x 1 = 5 Marks)

1. C4 stands for

   (a) Controlled Collapsed Chip Connection (b) Chip Connection Called Contact

   (c) Collapsed Chip Connect Confirmed (d) Connection Collapsed Chip Contact

2. Simulated annealing and evolution belong to

   (a) Integral class of algorithms

   (b) Probabilistic and iterative class of algorithms

   (c) Random and stochastic process of algorithms

   (d) Differential class of algorithms

3. Maze routing is based on

   (a) Depth first search (b) Breadth first search

   (c) Topological search (d) None of the above

4. Clock tree doesn't contain following cell

   (a) Clock buffer (b) Clock inverter

   (c) AOI cell (d) None of the above

5. What is routing congestion in the design?

(a) Ratio of required routing tracks to available routing tracks

(b) Ratio of available routing tracks to required routing tracks

(c) Depends on the routing layers available

(d) None of the above

PART - B (5 x 3 = 15 Marks)

6. List the basic NMOS design rules.

7. What is simulated annealing?

8. Write short notes on integer linear programming.

9. List the issues in minimization.

10. Differentiate 1D compaction and 2D compaction.

PART - C (5 x 16 = 80 Marks)

11. (a) Explain in detail the cell generation using PLA transistor chaining. (16)

Or

(b) With suitable diagrams, briefly discuss the layout methodologies. (16)

12. (a) Explain in detail the various floor planning techniques with neat diagrams. (16)

Or

(b) List the various placement algorithms and discuss any two in detail. (16)

13. (a) Give a detailed account of switch box routing algorithms in FPGA. (16)

Or

(b) With suitable diagrams explain

(i) Maze running (8)

(ii) Steiner tress (8)

14. (a) Explain in detail the various ways clock skew can be minimized. (16)

Or

(b) Explain in detail about constrained via minimization problem. (16)

15. (a) Discuss about the wire length and bend minimization techniques. (16)

Or

(b) Explain in detail

(i) Multiple chip modules (8)

(ii) Wein burger arrays (8)

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