**Reg. No. :** | | | | | | | | | | |

**Question Paper Code: 92073**

M.E. DEGREE EXAMINATION, APRIL 2015.

Elective

VLSI Design

01PVL519 – SYSTEM DESIGN USING FPGA

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Differentiate FPGA and CPLD.
2. Write the FPGA design flow.
3. What is slice, configurable logic blocks and look up table?
4. List the technology issues in FPGAs.
5. What are the different types of timing verification?
6. What is synthesis?
7. What do conditional assignments get inferred into?
8. List the synthesizable and non-synthesizable constructs.
9. When DFT and formal verification are used?
10. What is the significance of signature analysis?

PART - B (5 x 14 = 70 Marks)

11. (a) What are the programming techniques used in logic devices and FPGA? Illustrate any two techniques. (14)

Or

(b) What is the significance and design flow of CPLDs? Describe the CPLD architectures with necessary diagrams. (14)

12. (a) (i) Illustrate a typical configurable logic blocks used in the programmable logic for the FPGA. (7)

(ii) List the features of XC4000. Elucidate the simplified block diagram of XC4000 series configurable logic blocks. (7)

Or

(b) (i) Describe the configurable block used to bring signals into the chip and send them back again. (7)

(ii) Show how the configurable logic blocks are interconnected? (7)

13. (a) (i) What is the use of functional simulation? Write the recommendations to simulate your design. (7)

(ii) Write the steps for synthesizing the FPGA design. (7)

Or

(b) (i) Describe the simulation techniques to verify the timing. (7)

(ii) What is the significance of verification in FPGA design flow? Write the essential steps of the verification. (7)

14. (a) With the suitable example elucidate the various levels of modeling in FPGA. (14)

Or

(b) Describe the effectiveness of synchronous design with a suitable example. (14)

15. (a) Define testability? What is the use of testability measures? Describe the design for testability techniques to ensure that a device is testable. (14)

Or

(b) (i) What is the problem with BIST technique? Describe the method to overcome the problem with BIST technique. (7)

(ii) What are the types of formal verification methods used in FPGA? Explain the various formal verification methods with a suitable example. (7)

PART - C (1 x 10 = 10 Marks)

16. (a) Generate a pattern for 3-bit LFSR using BIST technique. (10)

Or

(b) Show how the logic blocks are used for designing a 4:1 multiplexer in XC5000 series. (10)