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Question Paper Code: 22071

M.E. DEGREE EXAMINATION, APRIL 2015.

Second Semester

VLSI Design

01PVL201-ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. What is meant by emitter injection efficiency and write its expression.
2. State the effect of substrate voltage on MOS device characteristics.
3. Draw the block diagram of self-biased reference circuit and its operation point determination characteristics curve.
4. Mention the need for short circuit current protection in integrated circuits.
5. List any two advantages of zero value time constant protection in integrated circuits.
6. Draw the circuit diagram for testing slew rate performance and write the expression for calculating output voltage.
7. Name the applications and the conditions for each application of Gilbert cell.
8. Mention the effect of reducing the loop filter bandwidth on PLL.
9. State the effect of channel length modulation on the current mirror ratio.
10. List any two drawbacks of MOS telescopic- cascade operational amplifiers.

PART - B (5 x 14 = 70 Marks)

11. (a) Derive the following parameters for the small signal low frequency model for a MOS transistor

(i) Transconductance (5)

(ii) Intrinsic gate- source and gate-drain capacitance (5)

(iii) Input and output resistance (4)

Or

(b) (i) An abrupt PN junction in silicon has densities N_A=10^{12} *atoms/cm*^{3} and N_D= 10^{13} atoms/cm^3. Calculate the junction built-in potential, the depletion layer depths, and the maximum field with 10 *V* reverse bias. (7)

(ii) With neat sketch enumerate the operation of substrate current flow in MOS transistors. (7)

12. (a) Draw the schematic of FET differential amplifier with active load and explain the effect of mismatch of g_m and R_d on the gain of differential amplifier. (14)

Or

(b) (i) Derive the expression of any one temperature independent biasing techniques and give its significance. (7)

(ii) Illustrace Class – B push pull output stage and draw its transfer characteristics. (7)

13. (a) Analyse the various methods of improving slew – rate in two stage bipolar and MOS Op – Amps. (14)

Or

(b) Explain the frequency response characteristics of any one single – stage amplifier with relevant expression. (14)

14. (a) Draw a four quadrant multiplier circuit using Gilbert cell and explain the method of improving input voltage range on V_2 input. (14)

Or

(b) With schematic and expression explain the operation of phase – locked loop in the locked condition and draw its frequency response curve. (14)

15. (a) What is the necessity of current mirrors in MOS technology and explain any two current mirror techniques in detail. (14)

Or

(b) (i) With neat schematic analyse the characteristics of telescopic operational amplifier. (7)

(ii) Draw the circuit of MOS folded cascade operational amplifier and explain its working principle. (7)

PART - C (1 x 10 = 10 Marks)

16. (a) Analyse the noises present in operational amplifiers and give the techniques to reduce input noise current. (10)

Or

(b) With neat constructional diagram and transfer characteristics explain the operation of NMOS devices on both enhancement and depletion region. (10)

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