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Question Paper Code: 42254

M.E. DEGREE EXAMINATION, MAY 2015.

Second Semester

POWER ELECTRONICS AND DRIVES

14PPE204 – DIGITAL CONTROLLERS IN POWER ELECTRONICS APPLICATIONS

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (5 x 1 = 5 Marks)

1. How many indirect memory addressing options are possible in C2XX series?

   (a) 6 (b) 5 (c) 4 (d) Infinity

2. If the Interrupt Enable (IE) bit is set

   (a) Peripheral generates an interrupt request to the PIE controller by asserting it PIRQ.

   (b) CPU interrupt request of the same priority level (INTn)

   (c) CPU stops what it is doing, masks all other maskable interrupts by setting the INTM bit

   (d) None of the above

3. Mapping address for auto sequence status register is

   (a) 70A8h (b) 70A7h (c) 70A6h (d) 70A5h

4. Which type of memory feature's in CPLD

   (a) Volatile (b) Non volatile (c) EPROM (d) Volatile EPROM

5. A controlled rectifier with a DC shunt motor as a load is driving a shaft connected to a conveyer belt, what happens, when the duty ratio of the rectifier is increased

   (a) Speed increases (b) Speed decreases

   (c) Increases initially then gradually decreases (d) No Change

PART - B (5 x 3 = 15 Marks)

6. Write some of the advanced features of LF2407.

7. Justify the cause of Non –Maskable Interrupt (NMI).

8. Describe the need for ADC Sequencer and write its various modes of operation.

9. Reproduce the fully populated condition in antifuse based programmable interconnect.

10. List out the various digital control methods in induction motor.

PART - C (5 x 16 = 80 Marks)

11. (a) (i) Explain the various memory addressing modes of TMS320LF2407 DSP Processor. (10)

(ii) Draw the general architecture of 240xA devices. (6)

Or

(b) Write a short note on the following with respect to TMS320LF2407 DSP Processor

(i) On-Chip RAM

(ii) Flash Control Mode Register

(iii) Program Memory

(iv) Data Memory (16)

12. (a) With a neat block diagram, explain about the Peripheral Interrupt Expansion (PIE) controller. (16)

Or

(b) Write in detail about the general purpose I/O control registers of TMS320LF2407 DSP Processor. (16)

13. (a) Draw and explain the basic functional blocks of event manager with necessary diagram. (16)

Or

(b) Discuss the following

(i) Features of capture units. (8)

(ii) Quadrature enclosed pulse circuit. (8)

14. (a) (i) Summarize the functions of flip flops inside the Configurable Logic Blocks (CLB) of Xilinx XC3000 series FPGA. (12)

(ii) Classify the various types of FPGA architecture. (4)

Or

(b) Sketch and explain the block diagram of Xup Virtex-II Pro FPGA development system and write its board components. (16)

15. (a) Design a VHDL program for a fully controlled rectifier and formulate the digital firing control logic to get a desired output DC voltage. (16)

Or

(b) Design a VHDL program for a PWM inverter and formulate the digital firing control logic to get a desired output AC voltage. (16)

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