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Question Paper Code: 42231

M.E. DEGREE EXAMINATION, MAY 2015.

Second Semester

Computer Science and Engineering

14PCS202 - MULTI CORE ARCHITECTURE

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (5 x 1 = 5 Marks)

1. An _____ dependence occurs when instruction i and instruction j, Write the same register or memory location
   (a) Output (b) Anti (c) Overcoming (d) Name

2. Cache coherence is _____.
   (a) Two processors can have two different values for the same memory location
   (b) Migration
   (c) Directory based
   (d) Snooping

3. CMP is _____
   (a) Chip level multiprocessing
   (b) Integrates two / more independent core memories
   (c) Multiple core CPU
   (d) Chip multithreading

4. 3Cs of cache miss are _____.
   (a) compulsory, capacity, conflict (b) control, capacity, coherence
   (c) cubic sensitivity, cores, confidence (d) confusion, capability, coding

5. Synchronous bus implies_____
   (a) Including clock in the control lines
   (b) Having fixed protocol for sending address not relative to clock
   (c) Running very fast
   (d) None of the above

PART - B (5 x 3 = 15 Marks)

6. State the approaches to exploit ILP.

7. What are the components of software pipeline loop?

8. What is message passing multiprocessor?

9. What is the need for cache memory?

10. What is software multithreading?

PART - C (5 x 16 = 80 Marks)

11. (a) Describe how instruction level parallelism is implemented. State the challenges. How are they attempted? (16)

Or

(b) What is multicore processor? Explain the need for multicore architecture? Discuss the salient features of CMP architecture in detail. (16)

12. (a) Describe symmetric and distributed shared memory architecture and their performance comparison. (16)

Or

(b) Explain memory consistency models and describe interconnection structures. (16)

13. (a) How the heterogeneous architectural issues are solved while implementation? Describe the typical architecture with functional components. (16)

Or

(b) Explain SUN CMP architecture and how the implementational challenges are addressed? (16)

14. (a) Explain the memory techniques suitable for multicore environment and how the optimization issues are handled? (16)

Or

(b) Explain the concept of virtual machines and virtual memory. Describe their issues in memory hierarchy of multicore systems. (16)

15. (a) What are the parallel programming models suitable for multi core programming? Explain shared memory programming. (16)

Or

(b) Write short notes on

(i) Message Passing Interface (8)

(ii) Open MP program development (8)
