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Question Paper Code: 31056

B.E. / B.Tech. DEGREE EXAMINATION, OCTOBER 2014.

Third Semester

Electronics and Instrumentation Engineering

01UEI306 - DIGITAL ELECTRONICS

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Convert the octal number 360.15 to decimal number.
2. Determine the XS3 equivalent of the following decimal number
   (a) 345 (b) 698.
3. Suggest a solution to overcome the limitation on the speed of the adder.
4. Implement the given function using NAND gates $F(x, y, z) = \sum m(0, 6)$.
5. How a D flipflop is converted into T flipflop.
6. Design a 3 bit Ring counter.
7. Differentiate fundamental mode and pulse mode asynchronous sequential circuits.
8. How do you eliminate the static 0 hazards?
9. Draw the logic diagram of static RAM cell and Bipolar RAM cell.
10. Define memory decoding.

PART - B (5 x 16 = 80 Marks)

11. (a) (i) Define the laws of Absorption. (2)

(ii) Simplify the logic function F(A,B,C,D) = ∏(3, 5, 6, 11, 13, 14, 15) using K - map in SOP and POS form. (10)

(iii) Convert the function F(A, B, C) = ∑m(1, 2, 6, 7) to canonical POS form. (4)

Or

(b) Simplify the function F = ∑(0, 1, 2, 3, 5, 9, 11) + d(4, 7, 15) using Quine Mclusky method and verify the result by K - map. (16)

12. (a) (i) Design a Full adder circuit using gates. (4)

(ii) Implement the following 3 variable Boolean functions using 4:1 MUX
F= ∑m(0, 2, 4, 5, 6, 7) (6)

(iii) Give the list of characteristics of TTL logic family. (6)

Or

(b) (i) Design a 3 bit binary to reflected code converter. Draw the logic diagram. (8)

(ii) Design a 3 bit magnitude comparator and draw the circuit. (8)

13. (a) Design a sequence detector to detect the sequence "01110" using D Flipflops (one bit overlapping). (16)

Or

(b) Design a sequential circuit using D Flipflops. Assume two inputs are A and B, outputs of the sequential circuit are outputs of D flipflops, present state = S, next state = s^*. consider the four states of the sequential circuit are S_0 = 00, S_1 = 01, S_2 = 10, S_3 = 11. (16)

Present State(S)	**Inputs(AB)**			
S_0	S_1	S_0	S_0	S_1
S_1	S_2	S_0	S_0	S_2
S_2	S_3	S_0	S_0	S_3
S_3	S_1	S_0	S_0	S_1

14. (a) Design an asynchronous sequential circuit for the following behavior. The circuit has two inputs A and B and two outputs O_0 and O_1. When both inputs are 0, outputs O_0 and O_1 are 0 and $Q^* = Q$. when both inputs are 1, outputs O_0 and O_1 are 1 and $Q^* = Q$. If Q = 0, either A = 1 or B = 1, output $O_0 = 0$ and $O_1 = 1$ and $Q^* = Q$. If Q = 1, either A = 1 or B = 1, output $O_0 = 1$ and $O_1 = 0$ and $Q^* = Q$. (16)

Or

(b) (i) Write short notes on races and hazards that occur in asynchronous circuits. (8)

(ii) Discuss the method used for race free assignment with example. (8)

15. (a) (i) Discuss memory organization with example. (4)

(ii) Implement the BCD to XS3 code conversion using ROM. (12)

Or

(b) (i) Draw the block diagram of a PLA and explain its architecture. (6)

(ii) Design a 2 bit comparator using PLA. (10)