Reg. No. : | | | | | | | | | | |

Question Paper Code: 92071

M.E. DEGREE EXAMINATION, OCTOBER - 2014.

Elective

VLSI Design

01PVL505 – GENETIC ALGORITHMS AND THEIR APPLICATIONS

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Write the need of genetic algorithm for VLSI design.
2. Define schema and macro cell.
3. List the available EDA tools for VLSI design.
4. What is multi way partitioning?
5. Write the advantages of hybrid GA.
6. How the genetic encoding is used to design IC_s?
7. What is meant by FPGA technology mapping?
8. List the Test generation procedures.
9. How do you estimate power in IC design?
10. Compare the GA and conventional algorithms.

PART - B (5 x 14 = 70 Marks)

11. (a) (i) State the steady state genetic algorithm. (4)

(ii) Give a detailed account of genetic operators. (10)

Or

(b) (i) Estimate the evaluation function of the fitness scaling algorithm. (7)

(ii) Illustrate the role of inversion operator in GA. (7)

12. (a) Explain the concept of automatic routing with its various approaches. (14)

Or

(b) Briefly discuss the partitioning algorithm with suitable examples. (14)

13. (a) (i) Write the role of local improvement in hybrid genetic algorithms. (7)

(ii) Discuss the weighted DFS reordering in detail. (7)

Or

(b) Explain the GASP algorithm for standard cell placement with an example. (14)

14. (a) Give a detailed account of macro cell global routing. (14)

Or

(b) Discuss the test generation in a GA frame work. (14)

15. (a) Explain the process of peak power estimation using GA. (14)

Or

(b) Give a detailed account of the implementation of parallel genetic algorithms for ATGS. (14)

PART - C (1 x 10 = 10 Marks)

16. (a) Discuss in brief about the taxonomy of partitioning algorithms. (10)

Or

(b) Explain the unified algorithm in detail. (10)

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