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Question Paper Code: 22071

M.E. DEGREE EXAMINATION, OCTOBER 2014.

Second Semester

VLSI Design

01PVL201-ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

(Regulation 2013)

Duration: Three hours

Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. What is punch through in MOS device? How it can be eliminated?
2. Draw the Small Signal Model of BJT.
3. What is the necessary condition for biasing?
4. What are the advantages of using push pull output stages?
5. Define Slew rate and justify its importance in OP AMP.
6. Define CMRR.
7. Define lock in range and capture range of a PLL.
8. Explain the roll of phase detector in Multiplier cell.
9. Compare cascode current mirror and folded cascode current mirror.
10. What are the advantages of class AB output stage?

PART - B (5 x 14 = 70 Marks)

11. (a) (i) Draw the Small Signal model of MOSFET and explain in detail. (10)
(ii) Explain briefly the capacitive effects present in MOSFET . (4)

Or

- (b) (i) Discuss the Short Channel effect in MOS transistors. (10)
(ii) What are the effects of weak inversion in MOS transistor? (4)
12. (a) (i) Discuss about the differential amplifier with active load using FET. (10)
(ii) Draw the band gap reference circuit and explain. (4)

Or

- (b) (i) Explain the push- pull output stage with neat diagram. (10)
(ii) An abrupt PN junction in silicon has doping $N_A = 10^{15}$ atoms/cm³ and $N_D = 10^{16}$ atoms/cm³. Calculate the junction potential. (4)
13. (a) (i) Discuss and analyze the slew rate model of OP amp. (10)
(ii) Write notes on OP AMP noise. (4)

Or

- (b) Discuss about the frequency response of multi stage amplifier in detail with performance analysis. (14)
14. (a) Explain the DC analysis of Gilbert Multiplier Cell and justify how it acts as an Analog Multiplier. (14)

Or

- (b) Explain in detail about the closed loop analysis of PLL. (14)
15. (a) Explain (i) Widlar current source. (7)
(ii) Wilson current source. (7)

Or

- (b) Explain in detail about MOS telescopic – cascode operational amplifier. (14)

PART - C (1 x 10 = 10 Marks)

16. (a) Sketch the cross section of a bipolar transistor and derive the equations to obtain the large signal characteristics. (10)

Or

- (b) Discuss the theory of Depletion region of PN junction with necessary equations in detail. (10)