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Question Paper Code: 12072

M.E. DEGREE EXAMINATION, DECEMBER 2014.

First Semester

VLSI Design

01PVL102 - ADVANCED DIGITAL SYSTEM DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Sketch the general form of synchronous sequential circuits.
2. Name the elements of ASM chart.
3. State any one condition for cause of race condition in ASC
4. What is the need for mixed operating mode circuits?
5. Identify any two common faults that can occur in PLA.
6. State the principle of Boolean difference method.
7. Write the classifications of PLDs.
8. State the programmable interconnect technology used in FPGA.
9. List the data types supported in VHDL.
10. Write the VHDL program for 2 – to – 1 Multiplexer.

PART - B (5 x 14 = 70 Marks)

11. (a) Design a clocked synchronous sequential network for a three-bit counter that counts the pulses on an input line, ‘W’. (14)

Or

(b) Develop ASM chart and circuit for the following application: The circuit has one input W and one output Z. All changes occur on the positive edge of the clock. If the input W is 1 for previous two clock cycles, the output Z is equal to 1, otherwise 0. (14)

12. (a) (i) Write short notes on the challenges in the design of asynchronous sequential circuit. (6)

(ii) Explain the causes for Static and Dynamic hazards in ASC. (8)

Or

(b) Explain the design of controller for a Vending machine of your choice. (14)

13. (a) (i) Explain the fault diagnosis using path sensitization with an example. (8)

(ii) Illustrate Test generation using DFT schemes. (6)

Or

(b) Explain the importance of creating Built in self test with an example. (14)

14. (a) Explain how any one code converter can be designed using PLA/PAL. (14)

Or

(b) Describe the architecture of logic block and PIA technology used in FPGA. (14)

15. (a) (i) Compare signals and variables. (6)

(ii) Write the VHDL code for 4 bit counter. (8)

Or

(b) (i) Illustrate behavioral modeling with an example. (6)

(ii) Write the VHDL code for 4 – to – 1 multiplexer. (8)

PART - C (1 x 10 = 10 Marks)

16. (a) Explain the features of Xilinx 4000 devices. (10)

Or

(b) Explain the various steps involved in Compact algorithm. (10)