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Question Paper Code: 41273

M.E. DEGREE EXAMINATION, DECEMBER 2014.

First Semester

VLSI Design

14PVL102 - ADVANCED DIGITAL SYSTEM DESIGN

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (5 x 1 = 5 Marks)

1. Digital hardware algorithms developed specifically are called as

   (a) Flow chart (b) ASM chart (c) State box (d) Decision box

2. What are the memory elements used in synchronous sequential circuits?

   (a) Unclocked flip flops (b) Time delay elements

   (c) Clocked flip flops (d) Feedback path

3. Which one is not a part of built in self test?

   (a) Pseudo random pattern generator (b) Tap controller.

   (c) Output Response Analyzer (ORA) (d) Build in block observer

4. _____ provides a programmable interface between the internal array of Logic.

   (a) CLB (b) IOB (c) CLL (d) PROM

5. In which process the construction of a gate level netlists from a model description in VHDL occur?

   (a) Synthesis (b) Translation (c) Routing (d) Technology mapping

PART - B (5 x 3 = 15 Marks)

6. List out the steps to analyse a Synchronous sequential circuit.

7. What are the three constraints that must be satisfied for an asynchronous sequential network to function properly?

8. What are the advantages of TMR/NMR scheme in fault tolerance?

9. Write a PLD program for reading a full adder using PAL.

10. Explain the concurrent and sequential statements in VHDL.

PART - C (5 x 16 = 80 Marks)

11. (a) Design a sequential network to convert BCD to Excess-3 code using Melay model. Also implement the circuit using a sequential PAL. (16)

Or

(b) Design an arithmetic circuit for adders which makes the fastest possible carry path circuit. Specify its worst delay. (16)

12. (a) Explain the following with a diagram.

(i) Data Synchronizer (8)

(ii) Mixed operating mode Asynchronous circuits (8)

Or

(b) Design an asynchronous sequential circuit that has two inputs x_2 and x_1 and one output z when x_1=0, the output z is 0. The first change in x_2 that occurs while x_1 is 1 will cause output z to be 1. The output z will remain 1 until x_1 returns to 0. (16)

13. (a) Discuss in detail about the D Algorithm with suitable examples. (16)

Or

(b) With an example circuit, explain how Fault Sensitization, Fault propagation and line justifications are performed in path sensitization method. (16)

14. (a) Design a 4-bit serial-in, serial-out shift register and implement it using suitable sequential PAL. (16)

Or

(b) (i) Explain the basic architecture of FPGA and its design methods . (10)

(ii) Write the PLD description for a 2 x 4 multiplexer. (6)

15. (a) (i) Explain the modeling of a J-K flip-flop in VHDL and give its code. (8)

(ii) Give the general block schematic of a Melay sequential machine. Explain the modeling approaches in VHDL for it. (8)

Or

(b) Design a 4 x 4 binary multiplier and write the VHDL code using behavioral model. (16)