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Question Paper Code: 21008

B.E. / B.Tech. DEGREE EXAMINATION, OCTOBER 2014.

Second Semester

Computer Science and Engineering

01UCS207- DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Realize OR gate using only NAND gates.
2. Subtract $(1010)_2$ from $(1000)_2$ using 2's complement method.
3. Convert the given number $(0110)_2$ into i) Gray code and ii) Excess-3 code.
4. Write a gate level HDL description for the full adder circuit.
5. Compare a Decoder with a De-multiplexer.
6. Determine the number of address lines required for accessing 2MB and a 64KB memory.
7. Show how a JK flip flop can be operated as a toggle flip flop.
8. State the differences between combinational logic and sequential logic.
9. What is a critical race? State its importance in an asynchronous sequential circuit.
10. List the assumptions that must be made for a fundamental mode circuit.

PART - B (5 x 16 = 80 Marks)

11. (a) (i) Simplify the following Boolean expression.

$$Y = \overline{A\overline{B} + ABC + A\,(B + A\overline{B})} \qquad (8)$$

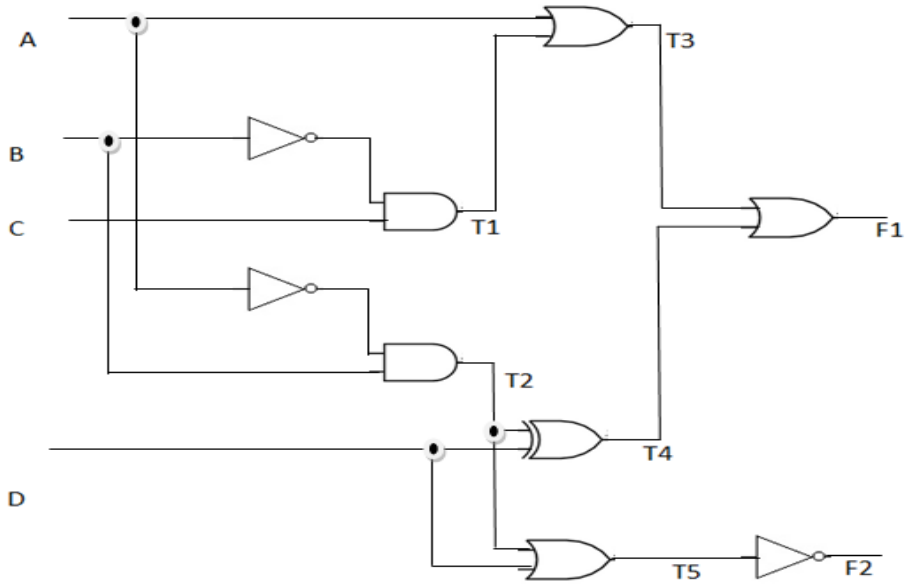
(ii) Simplify the following boolean function using K-map method.

$F\,(A,B,C,D,E) = \sum m\,(1,5,7,13,14,15,17,18,21,22,25,29) + \sum d\,(6,9,19,23,30)$ (8)

Or

(b) Find the minimal sum of products for the Boolean expression, $F\,(w,x,y,z) = \sum m\,(1,3,4,5,9,10,11) + \sum d\,(6,8)$ using Quine – Mc Cluskey tabulation method. (16)

12. (a) Analyze the combinational circuit shown in Fig. 12(a) to determine the boolean expressions and the truth table governing the outputs of the circuit.



(16)

Or

(b) (i) Design a combinational logic circuit to compare two 2-bit binary numbers A and B and to check whether A<B, A=B or A>B. (8)

(ii) Explain the BCD adder with a neat block diagram. (8)

13. (a) (i) Implement the function, F (A,B,C,D) = ∑m (0,1,2,5,6,9,12,14) using two 4x1 multiplexers. (8)

(ii) Write a structural Verilog description for a 2x4 decoder with a neat sketch.(8)

Or

(b) A combinational logic circuit is defined by the following functions:

F_1 (x,y,z) = ∑m (1,2,4,6)

F_2 (x,y,z) = ∑m (0,1,6,7)

F_3 (x,y,z) = ∑m (2,6)

F_4 (x,y,z) = ∑m (1,2,3,5,7)

Implement the circuit using a PLA with 3 inputs, 7 product terms and 4 outputs. (16)

14. (a) With suitable examples explain state reduction and state assignment of sequential circuits. (16)

Or

(b) (i) Design a 3 bit binary Up Counter using JK flip flops. (10)

(ii) Write the HDL description of a T flip flop and a JK flip flop from D flip flop. (6)

15. (a) (i) Discuss the need and operation of a De-bounce circuit with a neat diagram. (6)

(ii) Determine whether the circuit in Fig. 15(a) has a static hazard or not. If yes, design a hazard free logic for the same input and output relation.

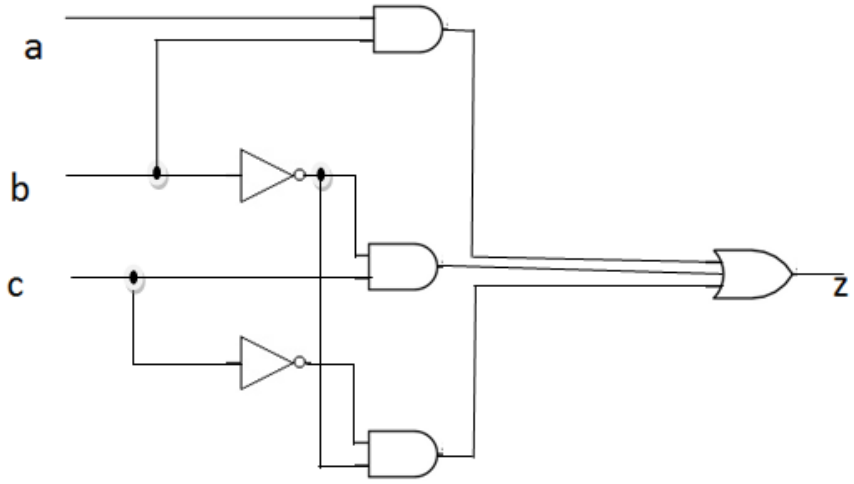


Fig. 15(a) (16)

Or

(b) (i) Briefly describe about race free assignment in asynchronous sequential circuits. (8)

(ii) Write short notes on hazards in combinational and sequential circuits. (8)