Reg. No. : | | | | | | | | | | |

Question Paper Code: 12071

M.E. DEGREE EXAMINATION, MAY 2014.

First Semester

VLSI Design

01PVL102 - ADVANCED DIGITAL SYSTEM DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Differentiate between state table and excitation table.
2. Draw ASM diagram for mod-8 binary counter.
3. What are races and cycles?
4. List the importance of data synchronizers.
5. What is stuck- at fault?
6. What is the significance of using BIST in digital circuits?
7. What is the need for programmable interconnect point?
8. List the difference between PLA and PAL.
9. What is a concurrence statement? Give one example.
10. Write down the VHDL code for a half adder.

PART - B (5 x 14 = 70 Marks)

11. (a) Design a BCD counter using state table assignment and reduction method. (14)

Or

(b) Explain the design of iterative circuits with an example. (14)

12. (a) Enumerate the design of asynchronous sequential circuit for eliminating static and dynamic hazards. (14)

Or

(b) Explain the design of vending machine controller. (14)

13. (a) (i) What is a fault? Explain Boolean difference method of fault diagnosis. (7)

(ii) Discuss compact algorithm. (7)

Or

(b) (i) Discuss the test generation by DFT scheme. (7)

(ii) Explain the path sensitization method. (7)

14. (a) Realize a full adder using PLA. (14)

Or

(b) With neat sketch, explain the operation of Xilinx XC4000 series. (14)

15. (a) Write a VHDL code to realise a 3 x 3 multiplier and a test bench to test its functionality. (14)

Or

(b) (i) Explain behavioral modeling with suitable example. (7)

(ii) Design a 4 bit parallel adder using VHDL. (7)

PART - C (1 x 10 = 10 Marks)

16. (a) For a suitable example, explain the design procedure using Algorithmic State Machines chart as design tool. (10)

Or

(b) Design a sequence recognizer for the following specifications. It is desired to produce a output '1' if and only if the current input and previous three inputs corresponds to either of the sequence "0110" or "1001". The output '1' is to occur at the time of the fourth input of the recognized sequence. Sequences should not overlap. (10)