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Question Paper Code: 92071

M.E. DEGREE EXAMINATION, MAY 2014.

Elective

VLSI Design

01PVL513 – DESIGNING WITH CPLDS AND FPGAS

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Decompose the function f (a, b, c) = ab + ac + bc.
2. Differentiate static and dynamic hazards.
3. What are the various steps for obtaining state assignment?
4. Compare Mealy and Moore machine.
5. What is meant by essential hafards?
6. State Unger's theorem.
7. Differentiate between PLA and PAL.
8. Draw the model of algorithmic state machine.
9. What are the different FPGA technologies?
10. Implement T-Flip-flop in FPGA.

PART - B (5 x 14 = 70 Marks)

11. (a) (i) Realize the following Boolean function using 8 - to - 1 line multiplexer where w, x and z appear on selection line S_2, S_1 and S_0 respectively

$f(w, x, y, z) = \sum m(1, 2, 6, 7, 9, 11, 12, 14, 15)$. (8)

(ii) Realize the following Boolean function using 3 - to - 8 - line decoder and NOR gates.

$F_1(x_2, x_1, x_0) = \sum m(0, 1, 5, 6, 7)$
$F_2(x_2, x_1, x_0) = \sum m(1, 2, 3, 6, 7)$. (6)

Or

(b) Determine all the static 1 - hazards and static 0-hazards for the following Boolean functions and redesign each network to be hazard-free.

$F_1(w, x, y, z) = yz + wxy' + w'yz'$
$F_2(w, x, y, z) = (w + x + y)(w + x' + z')(w' + x' + y')(w' + x + z)$. (14)

12. (a) The state table shown below is for a clocked synchronous sequential network. Assigning codes in binary order to the states, determine minimal-sum excitation and output expressions for the sequential network using JK flip - flop. (14)

Present state	Next state		Output(z)
	Input(x)		
	0	1	
A	A	B	1
B	C	A	0
C	A	D	0
D	C	C	1

Or

(b) Determine minimal state table for the following state table. (14)

Present state	Next state		Output(z)	
	Input(x)		Input(x)	
	0	1	0	1
A	B	C	1	1
B	D	B	0	0
C	B	A	0	1
D	D	E	0	0
E	F	G	1	1
F	D	F	0	0
G	F	H	0	1
H	F	I	1	1
I	B	E	0	1

13. (a) Design a fundamental mode asynchronous sequential network to meet the following requirements.

(1) There are two inputs x_1 and x_2 and a single output z.
(2) The inputs x_1 and x_2 never change simultaneously.
(3) The output is always to be 0 when $x_1 = 0$, independent of the x_2.
(4) The output is to become 1 if x_2 changes while $x_1 = 1$ and is to remain 1 until x_1 becomes 0 again. (14)

Or

(b) Implement the following using CPLD

(i) Shift Register.
(ii) Parallel Adder with accumulator. (14)

14. (a) Design PAL architecture to implement the following Boolean function

$F_1 (x, y, z) = \sum m (1, 2, 4, 6, 7)$
$F_2 (x, y, z) = \sum m (2, 4, 5, 6)$
$F_1 (x, y, z) = \sum m (1, 4, 6)$. (14)

Or

(b) Construct an ASM chart for a counter having a single input variable G. When G = 0, the counter is to behave as a mod - 8 binary counter; while when G = 1, it is to behave as a mod - 8 Gray - code counter. (14)

15. (a) Briefly explain XILINX 3000 series FPGA with necessary diagrams. (14)

Or

(b) Implement 4 - bit adder using XILINX FPGA. (14)

PART - C (1 x 10 = 10 Marks)

16. (a) Obtain a minimal state table for a clocked synchronous sequential network

having a single input line x, in which the symbols 0 and 1 are applied, and a single output line z. An output of 1 is to be produced coincident with each third multiple of the input symbol 1. At all other times the network is to produce 0 outputs.

X = 0 1 1 0 1 0 1 1 1 1 0 0 0 1 1 1 0
Z = 0 0 0 0 1 0 0 0 1 0 0 0 0 0 1 0 0. (10)

Or

(b) Design PLA architecture to implement the following Boolean function

$F_1 (x, y, z) = \sum m (3, 6, 7)$
$F_2 (x, y, z) = \sum m (0, 1, 2, 6, 7)$
$F_1 (x, y, z) = \sum m (0, 1, 3, 4, 5)$. (10)