Reg. No. : | | | | | | | | | | |

Question Paper Code: 22073

M.E. DEGREE EXAMINATION, MAY 2014.

Second Semester

VLSI Design

01PVL203 - LOW POWER VLSI DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. What are the sources of power consumption?
2. What are the limits of power?
3. List out the various techniques of power optimization.
4. What do you mean by logic level power optimization?
5. What are the special techniques adopted in the design of low power CMOS circuits?
6. What do you mean by a low power clock?
7. List the various power estimation techniques?
8. What is logic power estimation?
9. List any two synthesis tool for low power.
10. List any two approaches towards software power estimation.

PART - B (5 x 14 = 70 Marks)

11. (a) Explain the physics of power dissipation in CMOS FET devices. (14)

Or

(b) Describe the basic principle of low power design. (14)

12. (a) Explain the techniques for reducing power consumption in multipliers. (14)

Or

(b) Explain the method of low power design in circuit level. (14)

13. (a) Explain how the power consumption by memories is reduced. (14)

Or

(b) Describe the arithmetic technique for low power design. (14)

14. (a) Explain the logic power estimation technique in detail for combinational circuits. (14)

Or

(b) Explain the method of probabilistic power analysis. (14)

15. (a) Explain the behavior level transform for low power design. (14)

Or

(b) Explain the method of software design for low power. (14)

PART - C (1 x 10 = 10 Marks)

16. (a) Design a low power architecture for implementing a arithmetic logic unit. (10)

Or

(b) Explain how the interconnect and layout design helps in considerable reduction of power. (10)