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Question Paper Code: 22071

M.E. DEGREE EXAMINATION, MAY 2014.

Second Semester

VLSI Design

01PVL201-ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Write down the expression for the threshold voltage of an n-type MOS transistor by considering it as a four terminal device which involves the source to bulk voltage and the body effect co-efficient γ.
2. What is meant by "Weak Inversion" in MOS transistors.
3. Draw the emitter follower circuit and mention the advantage of this configuration.
4. What is the motivation to go for active loads in differential amplifiers.
5. Mention the causes of noise in OP-Amps.
6. Draw an ac schematic circuit of a common emitter amplifier and its equivalent circuit using Miller approximation.
7. Mention any two applications of an analog multiplier.
8. Draw the block diagram of a Phase Locked Loop system.
9. Draw a simple current mirror circuit using n-channel MOSFETs.
10. Draw the circuit of a MOS Widlar current source.

PART - B (5 x 14 = 70 Marks)

11. (a) (i) Explain the depletion region of a PN junction. (4)

(ii) Draw the basic small signal model of the bipolar transistor and derive the collector–base resistance and the collector–base capacitance. (10)

Or

(b) (i) Explain the large signal behaviour of a MOS transistor. (7)

(ii) Derive the drain current equation in the weak inversion state. (7)

12. (a) Explain the band gap reference bias circuits in CMOS technology to get temperature insensitive voltage references. (14)

Or

(b) With a neat circuit diagram, explain the behavior of self biasing for reducing the power-supply sensitivity. (14)

13. (a) Explain the frequency response of voltage buffers and write down the pole and zero of a source follower circuit. (14)

Or

(b) Explain the dominant-pole approximation of a multistage amplifier and derive the 3 dB frequency. (14)

14. (a) Explain the DC analysis of a Gilbert Multiplier Cell its use as an analog multiplier. (14)

Or

(b) A PLL has a K_o of 2π (1 kHz/V), a K_a of 500 s^{-1} and a free running frequency of 500 Hz.

(i) For a constant input signal frequency of 250 Hz and 1 kHz, find $V_{o.}$

(ii) Now the input signal frequency is modulated, so that

Find the output signal $V_0(t)$ (14)

15. (a) Explain the large signal analysis and small signal analysis of a differential pair with Current mirror load. (14)

Or

(b) Explain the MOS Active – Cascode Operational Amplifiers. (14)

PART - C (1 x 10 = 10 Marks)

16. (a) Explain the various MOS current sources used in low-current biasing. (10)

Or

(b) Explain the CMOS Class AB output stages with a neat diagram. (10)

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