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Question Paper Code: 22054

M.E. DEGREE EXAMINATION, MAY 2014.

Second Semester

Power Electronics and Drives

01PPE204 - DIGITAL CONTROLLERS IN POWER ELECTRONICS APPLICATION

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. With an example, indicate the accessing of memory operand using indirect addressing mode in motor control signal processor TMS320LF2407.
2. List the scaling shifters available in C2xx DSP controller.
3. Name the GPIO control registers of TMS320C2xx DSP.
4. What are the I/O multiplexing control registers?
5. List the trigger sources for DSP controller ADC.
6. What is meant by GP timer 1 underflow interrupt and GP timer 1 compare interrupt?
7. List out the advantages of FPGA.
8. What are the types of FPGA?
9. What are the merits of FPGA based control of PMSM?
10. What is micro-step mode in stepper motor?

PART - B (5 x 14 = 70 Marks)

11. (a) (i) Write TMS320LF2407 assembly language program to add two 16-bit data stored in the memory addresses 2000H and 2001H in the data memory and store the result in the data memory at addresses 3000H and 3001H. (7)

(ii) Explain the indirect addressing mode used to access memory in TMS320LF2407. (7)

Or

(b) (i) Explain about the components of C2xx DSP core. (10)

(ii) Discuss briefly about the physical memory available in TMS320LF2407 DSP. (4)

12. (a) Explain the different interrupt sources in TMS320LF2407 along with the function of various registers associated with the interrupts. (14)

Or

(b) Write notes on multiplexing and general purpose I/O control registers of DSP processor. (14)

13. (a) With a neat block diagram of event manager EVA explain the different sub-components in it in the TMS320LF2407. (14)

Or

(b) Describe the operation of the analog to digital converter of the DSP processor. (14)

14. (a) Describe with necessary diagrams about the configurable logic blocks (CLB) and programmable interconnect point (PIP) of FPGA processor. (14)

Or

(b) (i) Explain about IOB in FPGA. (7)

(ii) Write notes on CPLD vs FPGA. (7)

15. (a) Explain the algorithm for the generation of space vector PWM signals using the event manager in C2xx DSP processor. (14)

Or

(b) Explain the operations of FPGA based control implementation of DC-DC buck-boost converters. (14)

PART - C (1 x 10 = 10 Marks)

16. (a) Explain the application of FPGA control in PWM controlled induction motor as a case study. (10)

Or

(b) What is the necessity of digital control of controlled rectifier? Give VHDL codes for converter fed DC drive. (10)

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