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Question Paper Code: 12032

M.E. DEGREE EXAMINATION, MAY 2014.

Second Semester

Computer Science and Engineering

01PCS101 - COMPUTER ORGANIZATION AND DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. What is the significance of weighted execution time in measuring the performance of a computer?
2. What is name dependence?
3. Compare performance of a correlating branch predictor with that of a standard predictor.
4. Enumerate the main limitations of ILP.
5. What is software pipelining?
6. What are predicated instructions?
7. What is cache coherence?
8. What is the relaxed consistency model?
9. Define reliability, availability and dependability as applied to storage devices.
10. If a cache memory has a hit rate of 75%, memory references take 12 ns to complete if they hit in the cache and 100 ns on a cache miss, what is the average access time of the cache?

PART - B (5 x 14 = 70 Marks)

11. (a) (i) What are data hazards? (5)

(ii) Describe the different formats for encoding an instruction set. (9)

Or

(b) (i) Which are the main instructions for control flow? What is their significance in ISA? (8)

(ii) State and explain Amdahl's law. Give an example. (6)

12. (a) (i) A program has the following instruction mix:
45% Register-type, 15% loads, 15% stores, 10% jumps, 15% branches. In a 5 stage pipeline half the loads cause a load-use hazard, 25% of the branches are mispredicted and 50% of the jumps have their targets in the Branch Target Buffer. What is the average CPI of the program? The cycle time is 2 ns. What is the execution time of the program if it runs 1 Million instructions? (5)

(ii) Explain the concept of dynamic scheduling. (9)

Or

(b) (i) Explain in detail about the hardware speculation. (8)

(ii) Describe the working of a tournament predictor. (6)

13. (a) (i) Explain in detail about VLIW. (8)

(ii) Compare hardware and software speculation mechanisms. (6)

Or

(b) (i) How does global code scheduling help in achieving better ILP? (7)

(ii) Briefly explain about static branch prediction. (7)

14. (a) (i) Explain the snooping protocols for cache coherence. (8)

(ii) Discuss the design issues and performance of simultaneous multithreaded processors. (6)

Or

(b) (i) Bring out the major points of difference between symmetric and distributed shared memory architectures. (7)

(ii) Describe directory based cache coherence protocols. (7)

15. (a) (i) Describe the different RAID levels. (6)

(ii) How can miss rate of a cache be reduced? (8)

Or

(b) (i) Explain the techniques for reducing the cache miss penalty. (8)

(ii) How can we improve the main memory bandwidth? (6)

PART - C (1 x 10 = 10 Marks)

16. (a) With the help of a case study, discuss the software approaches used for ILP. (10)

Or

(b) Describe instances of the application of Amdahl's law in the design of computers. (10)