Reg. No. : | | | | | | | | | | |

Question Paper Code: 53036

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2017

Third Semester

Electrical and Electronics Engineering

15UEE306 - DIGITAL LOGIC CIRCUITS

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. The Gray code for decimal number 6 is equivalent to

   (a) 1100 (b) 1001 (c) 0101 (d) 0110

2. The digital logic family which has minimum power dissipation

   (a) TTL (b) RTL (c) DTL (d) CMOS

3. The gates required to build a half adder are

   (a) EX-OR gate and NOR gate (b) EX-OR gate and OR gate
   (c) EX-OR gate and AND gate (d) Four NAND gates

4. The Karnaugh map method of minimization of switching functions is very convenient and effective, if the number of variables in the switching function is

   (a) 8 (b) 4 (c) 5 (d) 6

5. For JK flip flop J = 0, K=1, the output after clock pulse will be

   (a) 1 (b) no change (c) 0 (d) high impedance

6. The output depends only on the present state of flip flops. this is a _____ circuit.

   (a) Moore (b) Mealy
   (c) Asynchronous (d) Feedback

7. Inputs at AND array are programmable and inputs at OR array are not programmable in

(a) PLA (b) PAL (c) FPGA (d) VHDL

8. Use of additional logic circuits in POS and SOP eliminates

(a) Static 0 hazards (b) Static 1 hazards
(c) Both a and b (d) None of these

9. In VHDL, which class of scalar data type represents the values necessary for a specific operation

(a) Integer types (b) Real types
(c) Physical types (d) Enumerated types

10. A wire in a circuit which is an output for another input in RTL model is called

(a) Constant (b) Variable (c) Signal (d) File

PART - B (5 x 2 = 10 Marks)

11. Reduce A'B'C' + A'BC' + A'BC.

12. State the limitations of Karnaugh map.

13. How does a latch differ from a flip flop?

14. Explain the procedure to obtain transition table.

15. What are the various modeling used in Verilog?

PART - C (5 x 16 = 80 Marks)

16. (a) (i) Explain about the error detection and correction codes used in the digital system while transmitting the binary information. (10)

(ii) Convert $(101011)_2$ into Gray code. (6)

Or

(b) Draw a two input TTL NAND gate with totem - pole output and explain its working. Give the static analysis when the output is low and high. Also summarize the characteristics of standard TTL. (16)

17. (a) Minimize the following logic function using K-maps and realize using NAND gate. $F(A, B, C, D) = \sum m(1, 3, 5, 8, 9, 11, 15) + d(2, 13)$. (16)

Or

(b) Design and Implement the following function using 8 to 1 multiplexer.
Y (A, B, C, D)= $\sum$ (0, 1, 2, 5, 9, 11, 13, 15). (16)

18. (a) With relevant diagram explain the working of a Master Slave JK flip flops and also explain its different state of working. (16)

Or

(b) Design a sequence detector circuit, which detects three or more consecutive 1's in a string of bits coming through an input line.
(a) Find the state diagram.
(b) Determine the type of the circuit (Moore or Mealy model).
(c) Tabulate state (or transition) table of sequence detector.
(d) Implement the circuit using D flip flop. (16)

19. (a) An asynchronous sequential circuit is described by the following excitation and output function. $Y = X_1 X_2 + (X_1 + X_2)Y$, $Z = Y$
(i) Draw the logic diagram of the circuit
(ii) Derive the transition table and output map
(iii)Describe the behavior of the circuit (16)

Or

(b) Elucidate the need for the PLds. Compare the logic construction of PROM, PLA and PAL. (16)

20. (a) Explicate about the design Strategies involved in the RTL Model with an example. (16)

Or

(b) Analyze the design units for a general sequential circuit. Draw a circuit consisting of logic state circuits , Seq C and Logic combinational circuit C which generates output Y. (16)
