Reg. No. : | | | | | | | | | | |

Question Paper Code: 53042

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2017

Third Semester

Electronics and Communication Engineering

15UEC302 - DIGITAL ELECTRONICS AND DESIGN

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 1 = 5 Marks)

1. Which of following are known as universal gates?

   (a) NAND & NOR (b) AND & OR (c) XOR & OR (d) None of these

2. The number of control lines for a 8 – to – 1 multiplexer is

   (a) 2 (b) 3 (c) 4 (d) 5

3. A Latch is _____ sensitive.

   (a) Both b and c (b) Edge (c) Level (d) None of these

4. In Moore models, output are function of only

   (a) Present State (b) Input State (c) Next State (d) Both a and b

5. The digital logic family which has minimum power dissipation is

   (a) TTL (b) RTL (c) DTL (d) CMOS

PART - B (5 x 3 = 15 Marks)

6. Define ‘minterm’ and ‘maxterm’.

7. Describe code converter? List their types.

8. Illustrate the logic diagram of a clocked SR flip flop.

9. Show the basic building blocks of an Algorithmic State Machine chart.

10. Distinguish between volatile and non-volatile memory.

PART - C (5 x 16 = 80 Marks)

11. (a) (i) State and prove De Morgan's theorems for 2-variables. (8)

(ii) Explain briefly about SOP and POS forms with example. (8)

Or

(b) (i) Develop the given function using K-map and obtain the simplified expression. $Y=\sum m(0, 2, 8, 10, 14)+\sum d(5, 15)$. (8)

(ii) Realize the functions of NOT, AND, OR and NOR gates only with NAND gates. (8)

12. (a) Design half adder and full adder and derive expression for sum and carry. Realize using logic gates. (16)

Or

(b) (i) How would you design a 3:8 decoder using basic gates. (8)

(ii) Deduce the design of a 1:4 demultiplexer circuit. (8)

13. (a) Explain the operation of master slave flip flop and show how the race around condition is eliminated in it. (16)

Or

(b) (i) Illustrate with diagram an asynchronous Up/Down counter & its operation with neat waveforms. (8)

(ii) Discuss the different types of shift registers with neat diagram. (8)

14. (a) (i) Draw the block diagram of an asynchronous sequential circuit and explain its operation. (8)

(ii) Explain the analysis of fundamental mode sequential circuit with an example.(8)

Or

(b) Discuss about static, dynamic and essential hazards in asynchronous sequential circuits with example. (16)

15. (a) Describe the internal organization of RAM and ROM with necessary diagrams. (16)

Or

(b) (i) Draw the internal construction of PLA having three inputs, four product terms and two outputs. (8)

(ii) Explain the architecture of FPGA with suitable diagrams. (8)