Reg. No. : | | | | | | | | | | |

Question Paper Code: 33042

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2017

Third Semester

Electronics and Communication Engineering

01UEC302 - DIGITAL ELECTRONICS AND DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. State Demorgan's theorem.
2. Find the complement of $A + BC + AB$.
3. What is data selector?
4. Define decoder.
5. Differentiate flip flop and latch.
6. Mention the problems faced by ripple counter.
7. What is the difference between PAL and PLA?
8. List the different types of memory.
9. Mention the steps involved in the design using ASM chart.
10. Compare synchronous and asynchronous sequential circuit.

PART - B (5 x 16 = 80 Marks)

11. (a) Using k-map method, obtain the minimal SOP and POS expressions for the function. $f(x, y, z, w) = \sum m(1, 3, 4, 5, 6, 7, 9, 12, 13)$. (16)

Or

(b) Simplify the following function using tabulation method.
$f(A, B, C, D) = \sum m(2, 3, 7, 9, 11, 13) + \sum d(1, 10, 15)$ (16)

12. (a) Design and implement an Excess – 3 to BCD code converter. (16)

Or

(b) Implement the following Boolean function using 16:1 multiplexer
$f(A, B, C, D, E) = \sum m(2, 4, 5, 7, 10, 14, 15, 16, 17, 25, 26, 30, 31)$. (16)

13. (a) List out the various types of shift registers. With neat diagram explain the Universal Shift register. (16)

Or

(b) Design a MOD-6 synchronous counter using J-K Flip-Flops. (16)

14. (a) With neat diagram explain the RAM organization. (16)

Or

(b) Narrate the operation of 2 input CMOS NAND and NOR gates. (16)

15. (a) Illustrate with an example the hierarchical modeling concepts used in Verilog HDL. (16)

Or

(b) Narrate the different types of Hazards. Discuss in detail how the hazards can be eliminated. (16)