Reg. No. : | | | | | | | | | | |

Question Paper Code: 53023

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2017

Third Semester

Computer Science and Engineering

15UCS303 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Common to Information Technology)

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 1 = 5 Marks)

1. The smallest entity of memory is called as

   (a) Cell (b) Block (c) Instance (d) Unit

2. To get the physical address from the logical address generated by CPU we use

   (a) MAR (b) MMU (c) Overlays (d) TLB

3. During transfer of data between the processor and memory we use

   (a) Cache (b) TLB (c) Buffers (d) Registers

4. Each stage in pipelining should be completed within ____ cycle

   (a) 1 (b) 2 (c) 3 (d) 4

5. The time lost due to branch instruction is often referred to as

   (a) Latency (b) Delay (c) Branch penalty (d) None of these

PART - B (5 x 3 = 15 Marks)

6. What are the different types of addressing modes available?

7. What are the difference between Stack and Queue?

8. What are the major characteristics of a pipeline?

9. What is DMA? Explain.

10. Differentiate Microprogrammed control from hardwired control.

PART - C (5 x 16 = 80 Marks)

11. (a) What are addressing modes explain different types of addressing modes. (16)

Or

(b) Differentiate between Horizontal and Vertical architecture. (16)

12. (a) What are Data hazards explain them. (16)

Or

(b) What is difference between 1's Complement and 2's Complement explain in detail. (16)

13. (a) Explain conversion of Floating point numbers into decimal and vise versa. (16)

Or

(b) Explain the techniques used to Measure and improve cache performance. (16)

14. (a) Explain pipeline in detail. (16)

Or

(b) Explain in detail on Memory hierarchy with examples. (16)

15. (a) What is cache memory explain its structure and working in detail. (16)

Or

(b) Explain the working of I/O interface in detail. (16)

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