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Question Paper Code: 31432

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2017

Third Semester

Electronics and Communication Engineering

01UEC302 - DIGITAL ELECTRONICS AND DESIGN

(Regulation 2013)

Duration: Three hours   Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. State Demorgan's theorem.

2. Realize EX-OR Gate from NAND Gate.

3. Write the truth table for full subtractor.

4. Define decoder.

5. Differentiate flip flop and latch.

6. What is the need of state minimization?

7. What is the difference between PAL and PLA?

8. List the different types of memory.

9. List the steps in the design of asynchronous sequential circuits.

10. Compare synchronous and asynchronous sequential circuit.

PART - B (5 x 16 = 80 Marks)

11. (a) Design a logic circuit using minimum number of basic gates for the Boolean expression $f = (A'B'C'D') + (A'B'C'D) + (A'B'CD') + (A'B'CD) + (A'BC'D') +$

(A'BC'D) + (A'BCD') + (AB'C'D) + (ABC'D') + (ABC'D) + (ABCD'). Use K map
to reduce the function. (16)

Or

(b) Simplify the following function using tabulation method and implement it using
universal gates. F (W, X, Y, Z) = Σ(1,2, 3, 5, 7,8, 13, 14,15). (16)

12. (a) Design and implement an Excess – 3 to BCD code converter. (16)

Or

(b) Explain the working of carry look ahead adder. (16)

13. (a) List out the various types of shift registers. With neat diagram explain the Universal
Shift register. (16)

Or

(b) Design a MOD-10 synchronous counter using J-K flip flops. Write the excitation
table and state table. (16)

14. (a) With neat diagram explain the RAM organization. (16)

Or

(b) Implement the following two Boolean functions
F1(A,B,C) = Σ(0,1,2,4)
F2(A,B,C) = Σ(0,5,6,7) using

i) PLA ii) PAL iii) ROM (16)

15. (a) Design an asynchronous sequential circuit with two inputs X and Y and with one
output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0, the output does
not change for any change in X. Use SR latch for implementation of the circuit.
(16)

Or

(b) What is a Hazard? What are the types of hazards? Check whether the following
circuit contains an hazard or not.

$Y = AB + \bar{B}C$

If the hazard is present, how to remove it. (16)

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