Reg. No. : | | | | | | | | | | |

Question Paper Code: 31464

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2017

Sixth Semester

Electronics and Communication Engineering

01UEC604 - VLSI DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. What is the objective of Layout rules?
2. List the various issues in Technology-CAD.
3. What is meant by crosstalk?
4. What is meant by design margin?
5. State the reasons for the speed advantage of CVSL family.
6. State any two criteria for low power logic design.
7. What is the need for testing?
8. What is mean by logic verification?
9. Mention the possible values which are allowed in Verilog HDL.
10. What are gate primitives?

PART - B (5 x 16 = 80 Marks)

11. (a) Explain in detail about ideal I-V characteristics and non-ideal characteristics of MOSFET. (16)

Or

(b) (i) With a neat diagram discuss in detail about DC transfer characteristics of CMOS inverter. (8)

(ii) Explain in detail about Ideal I-V characteristics of CMOS. (8)

12. (a) What is Power Dissipation? Explain the various ways to minimize the static and dynamic power dissipation. (16)

Or

(b) Discuss in detail about the resistive and capacitive delay estimation of the CMOS inverter circuit. (16)

13. (a) (i) Explain the issues related to the design of low power logic design. (8)

(ii) In short explain about static CMOS design. (8)

Or

(b) Explain in briefly about Synchronizers. (16)

14. (a) Describe in detail, the various manufacturing test principles in CMOS testing. (16)

Or

(b) Explain the method of boundary scan test in detail. (16)

15. (a) Write a Verilog HDL for an 8-bit ripple carry adder using structural model. (16)

Or

(b) Explain behavioral and gate level modeling with suitable example. (16)

———————