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Question Paper Code: 41404

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2017

Sixth Semester

Electrical and Electronics Engineering

14UEC624 - APPLIED DIGITAL SIGNAL PROCESSING

(Regulation 2014)

(Common to EIE and ICE branches)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. A ramp signal has

   (a) Infinite energy and zero power (b) Infinite energy and infinite power
   (c) zero energy and zero power (d) zero energy and infinite power

2. If a signal f(t) has energy E, the energy of the signal f(2t) is equal to

   (a) E (b) E/2 (c) 2E (d) 4E

3. If X(z) has a single on the unit circle, on negative real axis then, x(n) is

   (a) Signed constant sequence (b) Signed decaying sequence
   (c) Signed Growing sequence (d) Constant Sequence

4. If all poles of the system function H(z) have magnitude smaller than one, than the system will be

   (a) Stable (b) Unstable (c) BIBO stable (d) Both (a) and (c)

5. The phase factors are multiplied before the add and subtract operations in

   (a) DIT Radix 2 FFT (b) DIF Radix 2 FFT
   (c) Inverse DFT (d) Both (a) and (c)

6. When the DFT of a sequence x(n) is imaginary

(a) x(n) is real and even
(b) x(n) is imaginary and odd
(c) x(n) is real and odd
(d) x(n) is real

7. The relation between analog and digital frequency is nonlinear in case of

(a) Impulse invariant transformation
(b) Bilinear transformation
(c) Frequency sampling
(d) All the above

8. Symmetric impulse response having odd number of samples, N=7 with centre of symmetry α is equal to

(a) 2 (b) 5 (c) 3.5 (d) 3

9. The architecture that employs instruction level parallelism is

(a) Von Neumann architecture
(b) Harvard architecture
(c) Modified Harvard architecture
(d) VLIW architecture

10. The function of wait-state generator is

(a) To insert wait-state in internal and external bus cycles
(b) To insert wait-state in data memory cycles
(c) To insert wait-state in program memory cycles
(d) To insert wait-state in external bus cycles

PART - B (5 x 2 = 10 Marks)

11. Is the system y(n) = x(-n) time invariant or not.

12. State Parseval's relations in Z transform.

13. List any two properties of DFT.

14. What is the necessary and sufficient condition for linear phase characteristic in FIR filter?

15. What is pipelining?

PART - C (5 x 16 = 80 Marks)

16. (a) Show that unit impulse response can be used to obtain the response for any input for an LTI system. Also, determine whether the following systems are linear, time-invariant and causal.

(i) $y(t) = x(t/3)$
(ii) $y(n) = x(-n)$

(iii) $y(t) = x(t^2)$

(iv) $y(n) = x^2(2n)$ (16)

Or

(b) State and prove sampling theorem for low pass band limited signal and explain the process of reconstruction of the signal from its samples. (16)

17. (a) Using residue method find the inverse Z transform of

$X(z) = [1 + 3z^{-1}] / [(1 +3z^{-1}+2z^{-2})], |z| > 2.$ (16)

Or

(b) Find the frequency response of the following causal systems.

$y(n) = = \frac{1}{2} x(n)+x(n-1) +\frac{1}{2} x(n-2)$

$y(n)-\frac{1}{4} y(n-1)-\frac{3}{8} y(n-2)= x(n)+ x(n-1)$ (16)

18. (a) Derive 8 point radix 2 DIF-FFT algorithm with neat diagram. (16)

Or

(b) An 8-point sequence is given by x(n) = {2, 2, 2, 2, 1, 1, 1, 1} compute 8 point DFT of x(n) is given by Radix- 2 DIT-FFT. Also sketch the magnitude and phase spectrum. (16)

19. (a) Design a digital Butterworth filter with satisfying the constraints

$0.707 \leq |H(e^{j\omega})| \leq 1$ for $0 \leq \omega \leq \frac{\pi}{2}$

$|H(e^{j\omega})| \leq 0.2$ for $\frac{3\pi}{4} \leq \omega \leq \pi$

With T=1 sec using bilinear transformation. Realize the filter in each case using the most convenient realization form. (16)

Or

(b) Design a filter with $H_d(e^{j\omega}) = \begin{cases} e^{-j3\omega}, & \frac{-\pi}{4} \leq |\omega| \leq \frac{\pi}{4} \\ 0, & \frac{\pi}{4} < |\omega| \leq \pi \end{cases}$

Using a Hamming window with N = 7. (16)

20. (a) With a neat block diagram explain in detail about the architecture of TMS320C50. (16)

Or

(b) (i) Draw the block diagram of Harvard architecture of a DSP and explain its blocks. (8)

(ii) Explain various addressing modes of TMS processor. (8)

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