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Question Paper Code: 41464

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2017

Sixth Semester

Electronics and Communication Engineering

14UEC604 - VLSI Design

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. CMOS IC packages are available in

   (a) DIP configuration (b) SOIC configuration
   (c) DIP and SOIC configurations (d) Neither DIP nor SOIC configuration

2. _____ is ideally suited for applications using battery power or battery backup power.

   (a) MOS (b) P-MOS (c) N-MOS (d) CMOS

3. Which type of simulation mode is used to check the timing performance of a design?

   (a) Behavioral (b) Switch-level (c) Transistor-level (d) Gate-level

4. The time needed for an output to change as the result of an input change is known as

   (a) noise immunity (b) fanout (c) propagation delay (d) rise time

5. In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging and discharging of load capacitance?

   (a) Static dissipation (b) Dynamic dissipation
   (c) Both (a) and (b) (d) None of these

6. Before the commencement of design, the clocking strategy determines
   (a) Number of clock signals necessary for routing throughout the chip
   (b) Number of transistors used per storage requirement
   (c) Power dissipated by chip and the size of chip
   (d) All the above

7. Which among the following is regarded as an electrical fault?

   (a) Excessive steady-state currents (b) Delay faults
   (c) Bridging faults (d) Logical stuck-at-0 or stuck-at-1

8. Which types of stuck at fault model exhibits the reduced complexity level of test generation?

   (a) Single (b) Multiple
   (c) Both (a) and (b) (d) None of these

9. In VHDL, which object/s is/are used to connect entities together for the model formation

   (a) Constant (b) Variable (c) Signal (d) All the above

10. Among the VHDL features, which language statements are executed at the same time in parallel flow?

    (a) Concurrent (b) Sequential (c) Net-list (d) Test-bench

PART - B (5 x 2 = 10 Marks)

11. Define threshold voltage in CMOS.

12. What is the fundamental goal in Device modeling?

13. State time borrowing.

14. Define test access port.

15. What is the structural gate-level modeling?

PART - C (5 x 16 = 80 Marks)

16. (a) Explain layout design rules in detail. (16)

Or

(b) (i) Explain the DC transfer characteristics of CMOS inverter with necessary conditions for the different regions. (8)

(ii) Obtain the threshold voltage equation for different threshold voltage effects. (8)

17. (a) What are the various reliability problems associated with the failure of Integrated circuits? Explain elaborately with relevant diagrams. (16)

Or

(b) (i) Elaborate the influence of scaling on MOS device characteristics. (8)

(ii) With appropriate explanation obtain the expression for static and dynamic power dissipation of CMOS gates. (8)

18. (a) Explain in detail: (i) Conventional CMOS Latch (ii) Conventional CMOS Flip flop. (16)

Or

(b) Elaborate the design process of static CMOS. (16)

19. (a) What are the various testing methods to be considered while designing a VLSI circuit? (16)

Or

(b) (i) Explain Ad-Hoc testing and Built in soft test techniques. (8)

(ii) What are the challenges involved in silicon debugging? Explain. (8)

20. (a) Explain the concept involved in structural gate level modeling and also give the description for Decoder and parity encoder. (16)

Or

(b) Explain the concept of gate delay in VERILOG with example. (16)

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