Reg. No. : | | | | | | | | | | |

Question Paper Code: 31227

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2017

Second Semester

Computer Science and Engineering

01UCS207- DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Convert $(101101.1101)_2$ to decimal and hexadecimal form?
2. What are the limitations of K map?
3. Write down the truth table of a full subtractor.
4. Obtain the truth table for BCD to Excess -3 code converter.
5. Distinguish between a decoder and a demultiplexer.
6. Compare SRAM and DRAM.
7. Derive the characteristic equation of a JK flip flop.
8. What is a primitive flow table?
9. Define race condition.
10. Define hazards and its types.

PART - B (5 x 16 = 80 Marks)

11. (a) Reduce the following function using K-map technique and implement the reduced Boolean expression with basic gates

$f(A, B, C, D) = \pi M (0, 3, 4, 7, 8, 10, 12, 14) + d (2, 6)$. (16)

Or

(b) Minimize the expression using Quine McCluskey method (Tabulation) method $F=\sum m(0, 1,9, 15, 24, 29, 30)+\sum d(8, 11, 31)$. (16)

12. (a) Design a circuit that converts 8421 BCD code to Excess 3 code. (16)

Or

(b) (i) Design a full adder circuit with necessary diagram. (10)

(ii) Write the HDL description of the circuit specified by the following Boolean function. (6)

13. (a) Implement the following Boolean function using a 8 to 1 multiplexer F(A, B, C, D) = A'BD'+ ACD+ B'CD+ A'C'D. Also implement the function using 16 to 1 multiplexer. (16)

Or

(b) Implement the following function using PLA:

$A(x, y, z)= \sum m(1, 2, 4, 6)$

$B(x ,y, z)= \sum m(0, 1, 6, 7)$

$C(x, y, z)= \sum m(2, 6)$ (16)

14. (a) Design a synchronous counter which counts in the sequences 000, 001, 010, 011, 100, 101,110, 111,000 using D-FF. (16)

Or

(b) Implement T flip flop using D flip flop and JK flip flop. (16)

15. (a) Design an asynchronous sequential circuit with input X1 and X2 and one output Z. Initially and at any time if both the inputs are 0, output is equal to 0. When X1 or X2 becomes 1, Z becomes 1. When second input also becomes 1, Z=0; The output stays at 0 until circuit goes back to initial state. (16)

Or

(b) Implement the Switching Function $F=\sum m(1, 3, 5, 7, 8, 9, 14, 15)$ by a static hazard free two level AND OR gate network. (16)

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