Reg. No. : | | | | | | | | | | |

Question Paper Code: 41432

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2017

Third Semester

Electronics and Communication Engineering

14UEC302 – DIGITAL ELECTRONICS AND DESIGN

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. A(A+B) is same as

   (a) A (b) B (c) AB (d) A+AB

2. The simplified logic of the Boolean function $x'y'z + x'yz + xy'$ is

   (a) $x'yz+xyz$ (b) $x'z + xy'$ (c) $x'z'+ x'y'$ (d) $xz+xy$

3. The difference bit output of a half-subtractor is the same as

   (a) difference bit output of a full-subtractor
   (b) sum bit output of a half-adder
   (c) sum bit output of a full-adder
   (d) carry bit output of a half-adder

4. Which of the following is known as half-adder

   (a) XOR gate (b) XNOR gate (c) NAND gate (d) NOR gate

5. With a JK master slave flip-flop the master is clocked when the clock is

   (a) Low (b) High (c) Either Low or High (d) Constant

6. How many flip-flops are needed for a 4-bit counter?

   (a) 2 (b) 3 (c) 4 (d) 6

7. The voltage needed for a TTL IC power supply is

(a) 5V dc (b) 10 V dc (c) 2 V dc (d) 20 V dc

8. Which of the following memories in non-volatile memory?

(a) ROM (b) PROM
(c) Ferrite core memory (d) None of these

9. Hazards occurs in

(a) Sequential circuit (b) Combinational circuit
(c) Both (a) and (b) (d) None of these

10. In synchronous sequential circuits, the memory elements are

(a) unclocked flip-flops (b) clocked flip-flops
(c) Both (a) and (b) (d) None of these

PART - B (5 x 2 = 10 Marks)

11. Define Associative law and Distributive law.

12. Compare half adder & full adder.

13. Differentiate between Latch and Flip-flop.

14. Draw the circuit diagram of a TTL-NAND gate with totem pole output.

15. List the design procedure of Asynchronous sequential circuits.

PART - C (5 x 16 = 80 Marks)

16. (a) Consider the minimization of the following switching function using the QUINE-McCLUSKEY method. $F(x_1, x_2, x_3, x_4)=\sum(0, 5, 7, 8, 9, 10, 11, 14, 15)$. (16)

Or

(b) Simplify the following function in (a)SOP (b)POS

$F(A,B,C,D)= \Sigma(0,1,2,5,8,9,10)$. (16)

17. (a) Design and implement Binary to Gray code convertor. (16)

Or

(b) Draw and explain a binary half-adder. Find out its sum and carry bit outputs. Also show how it can realized using five NAND gates. (16)

18. (a) Explain the working of a positive edge triggered J-K flip flop with neat diagram. (16)

Or

(b) Explain the working of 3-bit universal shift register with neat block diagram. (16)

19. (a) Explain memory decoding. Compare the RAM, ROM, PROM and EPROM. (16)

Or

(b) (i) Differentiate registered PAL and configurable PAL (8)

(ii) Design a 4-bit binary–to gray code converter using PROM. (8)

20. (a) Explain how a state graph for a sequential machine can be convened to an equivalent ASM chart. (16)

Or

(b) Design a sequential pattern detector that receives a stream of input bits. The circuit should recognize the pattern 010 and produce an output whenever this pattern is received. (16)

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