Reg. No. :

Question Paper Code: 41536

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2017

Third Semester

Electronics and Instrumentation Engineering

14UEI306 - DIGITAL ELECTRONICS

(Regulation 2014)

Duration: Three hours

Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 1 = 10 Marks)

1. Sum of product can be implemented with a group of (a) NOT gates (b) OR gates (c) AND gates (d) XOR gates 2. Each square in a karnaugh map represents a (a) Points (b) Values (c) Minterm (d) Maxterm 3. How many 3-line-to-8-line decoders are required for a 1-of-32 decoder? (a) 1 (b) 2 (c) 4 (d) 8 4. A comparator is a special combinational circuit designed primarily to compare the relative magnitude of _____ numbers . (a) two decimal (b) three decimal (c) two binary (d) three binary 5. How is a J-K flip-flop made to toggle? (a) J = 0, K = 0(b) J = 1, K = 0(c) J = 0, K = 1(d) J = 1, K = 16. In a 6-bit Johnson counter sequence there are a total of how many states, or bit patterns. (d) 24 (a) 2 (b) 6 (c) 12

- 7. Race in which stable state depends on order is called
 - (a) critical race(b) identical race(c) non critical race(d) defined race
- 8. In design procedure of asynchronous circuit flow table is

| (a) increased to max states(c) changed | (b) reduced to min states(d) remain same |
|--|--|
| What is an OTP device? | |
| (a) Optical transporting port(c) Operational topical portable | (b) Octal transmitting pixel(d) One-time programmable |
| The storage element for a static RAM is | |
| (a) diode | (b) resistor |
| (c) capacitor | (d) flip-flop |

PART - B (5 x 2 = 10 Marks)

11. What are called don't care conditions?

9.

10.

- 12. Draw the logic Symbol and construct the truth table for the two input EX NOR gate.
- 13. List out the applications of Flip Flops.
- 14. What are the steps for the design of asynchronous sequential circuit?
- 15. What is programmable logic array? How it differs from ROM?

PART - C (5 x 16 = 80 Marks)

16. (a) Minimize the logic function $Y(A,B,C,D) = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$. Use Karnaugh map. Draw logic circuit for the simplified function. (16)

Or

(b) Using tabulation method simplify: $F(A, B, C, D, E) = \sum (0, 1, 4, 5, 16, 17, 21, 25, 29).$

(16)

17. (a) Draw the block schematic of Magnitude Comparator and explain its operations. (16)

Or

- (b) Design BCD adder and explain its working with necessary circuits. (16)
- 18. (a) Design a 3 bit Johnson counter and explain its operation. (16)

41536

| | (b) | Design a Moore type sequence detector to detect a serial input sequence of 101. | (16) |
|-----|-----|---|------|
| 19. | (a) | Explain with neat diagram the different hazards and the way to eliminate them. | (16) |
| | | Or | |
| | (b) | Explain the different methods of state assignment. | (16) |
| 20. | (a) | Explain with neat diagrams a RAM architecture. | (16) |
| | | Or | |
| | (b) | Explain in detail about PLA with a specific example. | (16) |