Reg. No. : | | | | | | | | | | |

Question Paper Code: 50534

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2017

Third Semester

Electronics and Instrumentation Engineering

15UEI304 - DIGITAL ELECTRONICS

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. What is the binary equivalent of the decimal number 368?

   (a) 101110000 (b) 110110000
   (c) 111010000 (d) 111100000

2. The decimal equivalent of hex number 1A53 is

   (a) 6793 (b) 6739 (c) 6973 (d) 6379

3. The NAND gate output will be low if the two inputs are

   (a) 00 (b) 01 (c) 10 (d) 11

4. The number of control lines for a 8 – to – 1 multiplexer is

   (a) 2 (b) 3 (c) 4 (d) 5

5. How many Flip-Flops are required for mod–16 counter?

   (a) 5 (b) 6 (c) 3 (d) 4

6. A ring counter consisting of five Flip-Flops will have

   (a) 5 states (b) 10 states (c) 32 states (d) Infinite states

7. The time required to change the input after the application of output is

(a) propagation delay (b) rise time
(c) fall time (d) peak time

8. Which one is the suitable to detecting the hazard in circuit?

(a) Logic gates (b) Karnaugh map
(c) Boolean expression (d) None of these

9. Which of the memory is volatile memory?

(a) ROM (b) RAM (c) PROM (d) EEPROM

10. In a RAM, information can be stored

(a) By the user, number of times (b) By the user, only once
(c) By the manufacturer, a number of times (d) By the manufacturer only once

PART - B (5 x 2 = 10 Marks)

11. Convert 0.640625 decimal numbers to its octal equivalent.

12. Implement the Boolean Expression for EX – OR gate using NAND Gates.

13. What is edge-triggered flip-flop?

14. Mention the significance of state assignment.

15. What is programmable logic array? How it differs from ROM?

PART - C (5 x 16 = 80 Marks)

16. (a) (i) Convert the binary number $(101111.1101)_2$ in to decimal. (8)

(ii) Design a 4 bit BCD to Excess-3 code converter. (8)

Or

(b) Obtain the minimum SOP using QUINE- McCLUSKY method and verify using K-map $(A,B,C,D) = \sum(1, 2, 3, 7, 8, 9, 10, 11, 14, 15)$ (16)

17. (a) Discuss in detail, the working of Full Adder logic circuit and extend your discussion to explain a binary adder, which can be used to add two binary numbers. (16)

Or

(b) With the help of a logic diagram and a truth table, explain a 3-line-to-8-line decoder using AND gates. (16)

18. (a) Define a register. Construct a shift register from S-R flip-flops. Explain its working. (16)

Or

(b) Design a MOD-6 synchronous counter using J-K Flip-Flops. (16)

19. (a) Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is one, input X is transferred to Z. When Y is zero, the output does not change for any change in X. (16)

Or

(b) Illustrate the concepts of hazards problem and explain the elimination methods. (16)

20. (a) Explain with neat diagrams a RAM architecture. (16)

Or

(b) Explain in detail about PLA with a specific example. (16)

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