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Question Paper Code: 41227

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2017

Second Semester

Computer Science and Engineering

14UCS207 – DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 1 = 10 Marks)

1. The output of an AND gate is LOW _____.
   (a) when any input is LOW (b) when any input is HIGH
   (c) when all inputs are HIGH (d) all the time
2. When used with an IC, what does the term "QUAD" indicate?
   (a) 4 circuits (b) 2 circuits (c) 8 circuits (d) 6 circuits
3. Which of the following expressions is in the sum-of-products (SOP) form?
   (a) AB + CD (b) AB(CD) (c) (A + B)(C + D) (d) (A)B(CD)
4. The systematic reduction of logic circuits is accomplished by:
   (a) symbolic reduction (b) using Boolean algebra
   (c) TTL logic (d) using a truth table
5. Boolean algebra is also known as
   (a) Gate algebra (b) Transistor algebra (c) Switching algebra (d) Counting algebra
6. 3 bits full adder contains
   (a) 3 combinational inputs (b) 4 combinational inputs
   (c) 6 combinational inputs (d) 8 combinational inputs

7. SR Flip flop can be converted to T-type flip-flop if?

(a) S is connected to Q (b) R is connected to Q
(c) Both S and R are shortened (d) S and R are connected to Q and Q' respectively

8. For which of the following flip-flop the output clearly defined for all combinations of two inputs?

(a) Q type flip-flop (b) R S type flip-flop
(c) J K flip-flop (d) T flip-flop

9. Combinations that are not listed for input variables are

(a) overflows (b) carry (c) dont cares (d) zero bits

10. If two systems have different codes then circuit inserted between them is

(a) sequential circuit (b) combinational circuit
(c) combinational sequence circuit (d) conversion circuit

PART - B (5 x 2 = 10 Marks)

11. Express the function Y =A+BC in canonical POS.

12. Explain the design procedure for combinational circuits.

13. Give the applications of Demultiplexer.

14. Define race around condition.

15. What is a state equation?

PART - C (5 x 16 = 80 Marks)

16. (a) (i) Find the Minimized logic function using K-Maps and Realize sing NAND and NOR gate. $F(A,B,C,D)= \sum m(1,3,5,8,9,11,15) + d(2,13)$ (8)

(ii) Show that if all the gate in a two-level OR-AND gate network are replaced by NOR gate, the output function does not change. (8)

Or

(b) How would you express the Boolean function using K-map and draw the logic diagram $F(w,x,y,z)= \sum m(0,1,2,4,5,6,8,9,12,13,14)$ (16)

17. (a) (i) Analyze the function of Binary multiplier with neat diagram. (8)

(ii) Develop a Full adder using decoder. (8)

Or

(b) Demonstrate 4-bit magnitude comparator with three outputs: A>B, A=B and A<B. (16)

18. (a) (i) Analyze the design of a 8 x 1 multiplexer using only 2 x 1 multiplexer. (8)

(ii) Formulate the following Boolean function using 4 x 1 multiplexers.

$F(A,B,C,D) = \sum(1,2,3,6,7,8,11,12,14)$ (8)

Or

(b) (i) How would you design a 3:8 decoder using basic gates? (8)

(ii) Deduce the design of a 1:4 Demultiplexer circuit. (8)

19. (a) (i) Construct and explain the working of a 4-bit Up/Down ripple counter. (8)

(ii) Model a synchronous MOD-5 counter and explain with waveforms. (8)

Or

(b) (i) Use T flip-flop to design counter with the following repeated binary sequence 0, 4, 7, 2, 3. (8)

(ii) Realize JK Flip Flop using SR Flip Flop. (8)

20. (a) (i) What is a Hazard? Give hazard free realization for the following Boolean function. $F(A, B, C, D) = \Sigma m(0, 2, 6, 7, 8, 10, 12)$. (8)

(ii) Find the ASM chart for binary multiplier. (8)

Or

(b) (i) What are static and dynamic hazards? Give static – 0 hazard free realizations for the following Boolean function. $F(A, B, C, D) = \Pi_M(3, 4, 5, 7, 9, 13, 14, 15)$. (8)

(ii) Write the design procedure for Asynchronous sequential logic circuits. (8)