Reg. No. : | | | | | | | | | | |

Question Paper Code: 41233

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2017

Third Semester

Computer Science and Engineering

14UCS303 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. The internal Components of the processor are connected by

   (a) Processor intra-connectivity circuitry (b) Processor bus
   (c) Memory bus (d) Rambus

2. In the following indexed addressing mode instruction, MOV 5(R1),LOC the effective address is

   (a) EA = 5+R1 (b) EA = R1 (c) EA = [R1] (d) EA = 5+[R1]

3. The processor keeps track of the results of its operations using a flags called

   (a) Conditional code flags (b) Test output flags
   (c) Type flags (d) None of these

4. In IEEE 32-bit representations, the mantissa of the fraction is said to occupy _____ bits.

   (a) 24 (b) 23 (c) 20 (d) 16

5. Each stage in pipelining should be completed within _____ cycle.

   (a) 1 (b) 2 (c) 3 (d) 4

6. If an exception is raised and the succeeding instructions are executed completely, then the processor is said to have

(a) Exception handling (b) Imprecise exceptions
(c) Error correction (d) None of these

7. When instruction i and instruction j are tends to write same register or memory location, it is called

(a) Input dependence (b) Output dependence
(c) Ideal pipeline (d) Digital call

8. Term which is named as shared memory with both SMP and DSM referring that address space is

(a) Multi-threading (b) Recurrence
(c) Dedicated (d) Shared memory

9. The extra time needed to bring the data into memory in case of a miss is called as

(a) Delay (b) Propagation time (c) Miss penalty (d) Data latency

10. Which interrupt is un-maskable?

(a) RST 5.5 (b) RST 7.5 (c) TRAP (d) Both a and b

PART - B (5 x 2 = 10 Marks)

11. State and explain the performance equation.

12. Write the multiply rule for floating point number.

13. List out the major characteristics of pipelining.

14. Define interleaved or fine grained multithreading.

15. Define the term memory mapped I/O.

PART - C (5 x 16 = 80 Marks)

16. (a) Explain the Eight ideas of the Computer architects in detail. (16)

Or

(b) Define addressing modes and explain the various addressing modes with the help of examples. (16)

17. (a) Derive and explain an algorithm for adding and subtracting two floating point binary numbers. (16)

Or

(b) Perform the integer division using non-restoring and restoring division 9 / 4. (16)

18. (a) State and explain the different types of hazards that can occur in a pipeline. (16)

Or

(b) Draw and explain the structure of a superscalar processor. Also explain the flow of instruction execution in it. (16)

19. (a) Discuss in detail instruction level parallelism. (16)

Or

(b) Explain Flynn's classification of computers. (16)

20. (a) Describe the basic operations of cache in detail with diagram and discuss the various mapping schemes used in cache design. (16)

Or

(b) Explain the virtual memory address translation and TLB with necessary diagram. (16)

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