| Reg. No.: | | | | | |
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Question Paper Code: 43602

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2018

Third Semester

Instrumentation and Control Engineering

| | 14 | 4UIC302 – DIGI | TAL LOGIC CIRCUI | ΓS AND DESIGN | | |
|----|-------------------|--------------------|----------------------------------------|--------------------------------------------------------------------------------------|----------|--|
| | | | (Regulation 2014) | | | |
| Du | ration: Three hou | | answer ALL Questions | Maximum: 10 |)0 Marks | |
| | | PAR | $ATA - (10 \times 1 = 10 \text{ Mag})$ | rks) | | |
| 1. | How many outpu | ats are on a BCD | decoder? | | | |
| | (a) 4 | (b) 16 | (c) 8 | (d) 10 | | |
| 2. | What are the syn | nbols used to rep | resent digits in the bin | ary number system? | | |
| | (a) 0,1 | (b) 0,1,2 | (c) 0 through 8 | (d) 1,2 | | |
| 3. | What is ROM? | | | | | |
| | (a) repeat on | memory | (b) read o | n memory | | |
| | (c) read only | memory | (d) repea | only memory | | |
| 4. | In PROM, we ca | n | | | | |
| | • | | | (b) store and erase data once(d) store once and read once | | |
| 5. | Which type of ga | ate can be used to | add two bits? | | | |
| | (a) Ex-OR | (b) Ex-N | VOR (c) Ex-NA | AND (d) NOR | | |
| 6. | How many flipfl | ops are required | to build a binary coun | er that counts from 0 to | 1023? | |
| | (a) 12 | (b) 20 | (c) 50 | (d) 10 | | |

| 7. | The next state variable | s in asynchronous so | equential circuits are called | d | | | |
|-----|--------------------------------------------------------------------|------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|--------------------------|--|--|--|
| | (a) secondary varia(c) primary variable | | (b) excitation variables(d) short term memory | | | | |
| 8. | In ASM, the decision be | ox is represented by | , | | | | |
| | (a) circle | (b) oval | (c) diamond | (d) rectangle | | | |
| 9. | Which of the following | logic family has the | e shortest propagation dela | y? | | | |
| | (a) CMOS | (b) NMOS | (c) ECL | (d) 74Sxx | | | |
| 10. | In VHDL, the mode of | a port does not defin | ne: | | | | |
| | (a) an input | (b) an output | (c) the type of the bit | (d) none of the above | | | |
| | | PART - B (5 | x 2 = 10 Marks) | | | | |
| 11. | List the different number | er systems? | | | | | |
| 12. | 2. Define fan in and fan out. | | | | | | |
| 13. | Compare combinationa | l and sequential circ | euits | | | | |
| 14. | What is race around con | ndition? | | | | | |
| 15. | List the advantages of C | CMOS logic. | | | | | |
| | | PART - C (5 x | x 16 = 80 Marks) | | | | |
| 16. | (a) Reduce the following | ng functions using I | ζ-map techniques. | | | | |
| | · · · · · · · · · · · · · · · · · · · | $= \sum_{n=1}^{\infty} m(0, 1, 2, 3, 5, 7)$ $= \prod_{n=1}^{\infty} M(0, 3, 4, 7, 8, 7)$ | 7, 8, 9, 11, 14) 10, 12, 14) + d (2, 6) | (8) (8) | | | |
| | | | Or | | | | |
| | (b) Use Quine–Mc $f(a, b, c, d) = \sum_{a} m(a, b, c, d)$ | cluskey method (0, 1, 2, 3, 8, 9). | d and simply the | following function, (16) | | | |
| 17. | (a) Design and draw 4 | bit binary to gray co | ode converter and explain. | (16) | | | |
| | | | Or | | | | |
| | (b) Explain in detail ab | out PLA with a spe | cific example. | (16) | | | |
| | | | | | | | |

| 18. | (a) | Design a four state down counter using T flip flop. | (16) |
|-----|-----|----------------------------------------------------------------------------------------------------------------------|------------|
| | | Or | |
| | (b) | Construct a decade ripple counter using flip flops and explain. | (16) |
| 19. | (a) | Draw the fundamental mode asynchronous circuit and explain in detail. | (16) |
| | | Or | |
| | (b) | (i) What is the procedure for obtaining the transition table form the circuit of an asynchronous sequential circuit? | diagram of |
| | | (ii) Discuss in detail the race conditions. | (8) |
| 20. | (a) | Explain the various modeling methods used in VHDL with an example. | (16) |
| | | Or | |
| | (b) | (i) Write VHDL code for a full sub tractor using logic Equation. | (8) |
| | | (ii) Write a VHDL description of an S-R latch using a process. | (8) |
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