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Reg. No. : | | | | | | | | | | |

Question Paper Code: 53306

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2018

Third Semester

Electrical and Electronics Engineering

15UEE306 - DIGITAL LOGIC CIRCUITS

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

PART A - (10 x 1 = 10 Marks)

1. The Gray code for decimal number 6 is equivalent to CO1- R

(a) 1100 (b) 1001 (c) 0101 (d) 0110

2. Convert the binary number 1001.0010_2 to decimal. CO1- R

(a) 90.125 (b) 9.125 (c) 125 (d) 12.5

3. Which of the following expressions is in the form of product of sums form CO2- R

(a) (A+B)(C+D) (b) (AB)+(CD)

(c) AB(CD) (d) AB+CD

4. How many AND gates are required to implement the Boolean expression, CO2- R

$X = AB\overline{C} + A\overline{B}C + \overline{A}BC$

(a) 1 (b) 2 (c) 3 (d) 4

5. On a master-slave flip-flop, when is the master enabled? CO3- R

(a) when the gate is LOW (b) when the gate is HIGH

(c) both of the above (d) neither of the above

6. A BCD counter is a _____. CO3- R

(a) binary counter (b) full-modulus counter

(c) decade counter (d) divide-by-10 counter

7. ASIC stands for: CO4 -R

(a) advanced speed integrated circuit.

(b) advanced standard integrated circuit.

(c) application specific integrated circuit.

(d) application speedy integrated circuit

8. Use of additional logic circuits in POS and SOP eliminates CO4 -R

(a) Static 0 hazards (b) Static 1 hazards (c) Both a and b (d) None of these

9. What is the basic difference between AHDL and VHDL? CO5 -R

(a) ADHL is used in all PLD's. (b) VHDL is used in all PLD

(c) ADHL is proprietary. (d)VHDL is proprietary.

10. In VHDL, the mode of a port does not define: CO5- R

(a) an input. (b) an output.

(c) both an input and an output. (d) the type of the bit

PART – B (5 x 2= 10Marks)

11. Reduce A'B'C' + A'BC' + A'BC. CO1 -R

12. Write the design procedure for combinational circuits? CO2 -R

13. Define race around condition. CO3 -U

14. What is programmable logic array? CO4- R

15. What are identifiers? CO5- R

PART – C (5 x 16= 80Marks)

16. (a) Explain about the error detection and correction codes used in the digital system while transmitting the binary information. CO1 -App (16)

Or

(b) (i) Explain Hamming code with an example. State its advantages over parity codes CO1 -App (16)
(ii) Design a TTL logic circuit for a 3-input NAND gate

17. (a) Simplify the Boolean function CO2 -App (16)
$F(w,x,y,z) = \sum m(0,1,2,4,5,6,8,9,12,13,14)$.

Or

(b) (i) Design an 8421 to gray code converter. CO2 -Ana (16)
(ii)Implement the Boolean function using 8:1 mux F (A, B, C, D) =A'BD'+ACD+B'CD+A'C'D.

18. (a) Using D-flip flop, design a synchronous counter which counts in the sequence 000, 001, 010, 011, 100, 101, 110, 111, 000. CO3- Ana (16)

Or

(b) Design a sequence detector circuit, which detects three or more consecutive 1's in a string of bits coming through an input line. CO3- Ana (16)
(a) Find the state diagram.
(b) Determine the type of the circuit (Moore or Mealy model)
(c) Tabulate state (or transition) table of sequence detector.
(d) Implement the circuit using D flip flop.

19. (a) Design an asynchronous sequential circuit that has 2 inputs x2 and x1, and one output z. the output is to remain 0 as long as an X1 is 0. The first change in x2 that occurs while x1 is 1 will cause z to be 1. Z is to remain 1 until x1 returns to 0. Construct a state diagram and flow table. Determine the output equations. CO4- U (16)

Or

(b) (i) A combinational circuit is defined by the functions. CO4 -Ana (16)

a. F1 (a, b, c) = $\sum$ m (3, 5, 6, 7)

b. F2 (a, b, c) = $\sum$ m (0, 2, 4, 7)

Implement the circuit with a PLA.

20. (a) Explain the design of Register Transfer Level (RTL) in VHDL. CO5- U (16)

Or

(b) Analyze the design units for a general sequential circuit. Draw a circuit consisting of logic state circuits , Seq C and Logic combinational circuit C which generates output Y. CO5- U (16)