Reg. No. : | | | | | | | | | | |

Question Paper Code: 43306

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2018

Third Semester

Electrical and Electronics Engineering

14UEE306 – DIGITAL ELECTRONICS

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. Convert hexadecimal value 16 to decimal.

   (a) 22 (b) 16 (c) 10 (d) 20

2. The propagation delay of TTL is

   (a) 10ns (b) 120ns (c) 200ns (d) None of these

3. The output of an exclusive-NOR gate is 1. Which input combination is correct?

   (a) A=1, B=0 (b)A=0, B=1 (c) A=0, B=0 (d) none of these

4. AND-OR realization is equivalent to

   (a) SOP (b) POS (c) K-map (d) None of these

5. Race around condition occurs in JK flip-flop if

   (a) J=1,K=1 (b) J=0,K=0 (c) J=0,K=1 (d) J=1,K=0

6. When the output of a sequential circuit depends on the present input as well as previous output states, the circuit is called

(a) Moore circuit (b) Mealy circuit (c) Sequential circuit (d) All of these

7. A PAL is

(a) Fixed OR and programmable AND
(b) Fixed OR and fixed AND
(c) Fixed AND and programmable OR
(d) Programmable OR and programmable AND

8. What programmable technology is used in FPGA devices?

(a) SRAM (b) FLASH (c) Antifuse (d) All the above

9. The example of sequential circuit is

(a) Counter (b) 7-segment display
(c) Combinational logic circuit (d) Shift register

10. The abbreviation of FSM is

(a) Finite state machine (b) Finite system model
(c) First system model (d) First state machine

PART - B (5 x 2 = 10 Marks)

11. Define fan-in and fan-out.

12. What is combinational circuit? Give examples.

13. Differentiate between Mealy and Moore models.

14. What is a hazard?

15. Write VHDL code for D flip-flop.

PART - C (5 x 16 = 80 Marks)

16. (a) (i) Convert the following

(a) $(764.352)_8$ to hexadecimal

(b) $(7A4.BA)_H$ to binary (8)

(ii) Explain Gray code and Binary code. (8)

Or

(b) (i) Convert 1010111011101100_2 into octal, decimal and hexadecimal equivalent. (8)

(ii) Explain Hamming code with an example. State its advantages over parity codes. (8)

17. (a) (i) Simplify the following function using Karnaugh map.

$f(w,x,y,z)=\sum(0,1,3,9,10,12,14)+\sum d(2,5,6,11)$ (8)

(ii) Implement the following function using only NAND gates.

$f(x,y,z)=\sum m(0,2,4,6)$ (8)

Or

(b) (i) Design a BCD to Excess-3 code converter. (8)

(ii) Design a full adder and implement it using suitable multiplexer. (8)

18. (a) Explain the circuit of a SRand JK flip-flop and explain its operation. (16)

Or

(b) (i) Design a serial adder using Mealy state model. (8)

(ii) List and explain the steps used for analyzing a synchronous sequential circuit. (8)

19. (a) Explain the various types of hazards in sequential circuit design and methods to eliminate them. Give suitable examples. (16)

Or

(b) (i) What are transition table and flow table? Give suitable examples. (6)

(ii) Implement the following function using PLA and PAL:

$f(x,y,z)=\sum m(0,1,3,5,7)$ (10)

20. (a) Write VHDL program for 4-bit ripple carry adder using structural modeling. (16)

Or

(b) Explain RTL design using VHDL with the help of examples. (16)