C **Reg. No. :** | | | | | | | | | | |

Question Paper Code: 53402

B.E./B.Tech. DEGREE EXAMINATION, MAY 2018

Third Semester

Electronics and Communication Engineering

15UEC302 -DIGITAL ELCTRONICS AND DESIGN

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

PART A - (5x 1 = 5 Marks)

Answer All Questions

1. Which of following are known as universal gates? CO1- R

   (a) NAND & NOR (b) AND & OR

   (c) XOR & OR (d) None of these

2. What is the equivalent gray code for the binary code 111? CO2-R

   (a) 101 (b) 100 (c) 000 (d) 001

3. Let $k = 2^n$. A circuit is built by giving the output of an n-bit binary counter as input to an n-to-2^n bit decoder. This circuit is equivalent to a CO3- R

   (a) k-bit binary up counter (b) k- bit binary down counter

   (c) k-bit ring counter (d) k-bit Johnson counter

4. How many flip flops are needed for a synchronous mod-3 counter? CO4- R

   (a) 3 (b) 4 (c) 1 (d) 2

5. Which of the following memories uses one transistor and one capacitor as basic memory unit? CO5-R

(a) SRAM (b) DRAM (c) Both SRAM and DRAM (d) None of the above

PART – B (5 x 3= 15Marks)

6. Prove that ABC + ABC' + AB'C + A'BC = AB + AC + BC. CO1-Ana

7. Define encoder and decoder CO2- U

8. What are the different types of shift registers? CO3- U

9. What are the steps for the design of asynchronous sequential circuit? CO4- U

10. Define RAM. Why RAMs are called as volatile? CO5- U

PART – C (5 x 16= 80Marks)

11. (a) Minimize the following function using Quine McCluskey method & verify the result using K-map method CO1-App (16)

$F(W, X,Y,Z) = \sum m(0,3,5,6,7,10,12,13) + \sum d(2,9,15)$

Or

(b) (i) Prove by perfect induction CO1 -App (8)

(1) (X + Y' + XY) (X + Y') (X'Y) = 0

(2) ABC + ABC' + AB'C + A'BC = AB + AC + BC

(3) A+A'B = A+B and

(4) A(A'+B) =AB

(ii) Draw the circuits of 2 input AND, OR, NOT, XNOR gates using NOR gate. CO1 -App (8)

12. (a) (i) Design a logic circuit that performs BCD to Excess-3 code conversion. CO2 -Ana (10)

(ii) Discuss about parity generator and parity checker. CO2 -Ana (6)

Or

	(b)	(i) Design half adder and full adder circuits.	CO2 -Ana	(8)
		(ii) Explain the operation of carry look-ahead adder with diagram.	CO2 -U	(8)
13.	(a)	(i) Draw the logic diagram of D-type edge triggered Flip Flop and explain its operation.	CO3- U	(8)
		(ii) Realize 1) JK Flip Flop from SR Flip Flop 2) T Flip Flop from JK Flip Flop	CO2 -Ana	(8)

Or

	(b)	With neat sketches, explain briefly the working of a universal shift register.	CO3- U	(16)
14.	(a)	Design an asynchronous sequential circuit that has two inputs X_2 and X_1 and one output Z. When X_1=0, the output Z is 0.The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain until X_1 returns to 0.	CO4-Ana	(16)

Or

	(b)	Explain the various types of hazards in sequential circuit design and the methods to eliminate them. Give suitable examples.	CO4 -U	(16)
15.	(a)	With a neat circuit diagram explain the operation of the following. (i) TTL NAND Logic (ii) CMOS NAND Logic.	CO5- U	(16)

Or

	(b)	Design using PAL the following Boolean functions: *(i) $W(A, B, C, D) = \Sigma(2, 12, 13)$* *(ii) $X(A, B, C, D) = \Sigma(7, 8, 9, 10, 11, 12, 13, 14, 15)$* *(iii) $Y(A, B, C, D) = \Sigma(0, 2,3, 4, 5, 6, 7, 8, 10, 11, 15)$* *(iv) $Z(A, B, C, D) = \Sigma(1, 2, 8, 12, 13)$*	CO5-U	(16)