Reg. No. : | | | | | | | | | | |

Question Paper Code: 43402

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2018

Third Semester

Electronics and Communication Engineering

14UEC302 – DIGITAL ELECTRONICS AND DESIGN

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. The equivalent hexadecimal of binary number 1011101.1011 is

   (a) B33 (b) EFF2.F (c) 5 D.B (d) 4A.67

2. The simplified logic of the Boolean function $x'y'z + x'yz + xy'$ is

   (a) $x'yz+xyz$ (b) $x'z + xy'$ (c) $x'z'+ x'y'$ (d) $xz+xy$

3. The logic required to decode the binary $(1011)_2$ by producing a HIGH indication on the output Y is

   (a) $Y = \bar{D}C\,\bar{B}\bar{A}$ (b) $Y= D\bar{C}\,BA$ (c) DC BA (d) $\bar{D}\bar{C}\,\bar{B}\bar{A}$

4. Which of the following is known as half-adder

   (a) XOR gate (b) XNOR gate (c) NAND gate (d) NOR gate

5. With a JK master slave flip-flop the master is clocked when the clock is

   (a) Low (b) High (c) Either Low or High (d) Constant

6. How many flip-flops are needed for a 4-bit counter?

   (a) 2 (b) 3 (c) 4 (d) 6

7. The voltage needed for a TTL IC power supply is

(a) 5V dc (b) 10 V dc (c) 2 V dc (d) 20 V dc

8. Which of the following memories in non-volatile memory?

(a) ROM (b) PROM
(c) Ferrite core memory (d) None of these

9. Hazards occurs in

(a) Sequential circuit (b) Combinational circuit
(c) Both (a) and (b) (d) None of these

10. In this mode the inputs and outputs are represented by levels

(a) Fundamental mode (b) Pulse mode
(c) Both (a) and (b) (d) None of these

PART - B (5 x 2 = 10 Marks)

11. Define Associative law and Distributive law.

12. Draw the 4-bit binary divider.

13. Differentiate between Latch and Flip-flop.

14. Draw the circuit diagram of a TTL-NAND gate with totem pole output.

15. List the design procedure of Asynchronous sequential circuits.

PART - C (5 x 16 = 80 Marks)

16. (a) Simplify the following expression using Quine Mccluskey method
f [w, x, y , z] = ∑ (0, 2, 3, 5, 6, 7, 8, 9) + d (10, 11, 12, 13, 14, 15)
Realize the minimized function using NOR gates only. (16)

Or

(b) Simplify the following function in (a)SOP (b)POS

F(A,B,C,D)= Σ(0,1,2,5,8,9,10). (16)

17. (a) (i) With logic diagram Truth table and explain about 3-to-8 decoder. (6)

(ii) Define multiplexer and implement the Boolean function with a suitable multiplexer. $F(A, B, C, D) = \Sigma$ (0, 1, 3, 4, 8, 9, 15). (10)

Or

(b) Draw and explain a binary half-adder. Find out its sum and carry bit outputs. Also show how it can realized using five NAND gates. (16)

18. (a) Explain the working of a positive edge triggered J-K flip flop with neat diagram. (16)

Or

(b) Explain the working of 3-bit universal shift register with neat block diagram. (16)

19. (a) Explain memory decoding. Compare the RAM, ROM, PROM and EPROM. (16)

Or

(b) (i) Differentiate registered PAL and configurable PAL (8)

(ii) Design a 4-bit binary–to gray code converter using PROM. (8)

20. (a) Explain how a state graph for a sequential machine can be convened to an equivalent ASM chart. (16)

Or

(b) Design an asynchronous sequential circuit that has two inputs x_1 and x_2 and one output z. The output z = 1 if x_1 changes from 0 to 1, z = 0 if x_2 changes from 0 to 1 and z = 0 otherwise. Realize the circuit using D FF. (16)