Reg. No. : | | | | | | | | | | |

Question Paper Code: 33402

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2018

Third Semester

Electronics and Communication Engineering

01UEC302 - DIGITAL ELECTRONICS AND DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. Use Boolean algebra to simplify the function $f = x(y + wz) + wxz$. Sketch the logic circuit for the minimized function using NAND gates.
2. Realize EX-OR Gate from NAND Gate.
3. Write the truth table for full subtractor.
4. Define decoder.
5. Differentiate the combinational logic from sequential logic.
6. What is the need of state minimization?
7. What is the difference between PAL and PLA?
8. List the different types of memory.
9. List the steps in the design of asynchronous sequential circuits.
10. Distinguish between Mealy and Moore state machines.

PART - B (5 x 16 = 80 Marks)

11. (a) Simplify the following expression $F(w, x, y, z) = \sum_m (1, 3, 4, 5, 9, 10, 11) + \sum_d (6, 8)$ using Quine – McCluskey method. (16)

Or

(b) Simplify the following function using tabulation method and implement it using universal gates. F (W, X, Y, Z) = Σ(1,2, 3, 5, 7,8, 13, 14,15). (16)

12. (a) Design and implement an Excess – 3 to BCD code converter. (16)

Or

(b) Explain the working of carry look ahead adder. (16)

13. (a) Explain the operation of D and T-flip flops. Write the truth table and draw their waveforms. Design the D and T-flip flops using JK flip flop. (16)

Or

(b) Design a MOD-10 synchronous counter using J-K flip flops. Write the excitation table and state table. (16)

14. (a) With neat diagram explain the RAM organization. (16)

Or

(b) Implement the following two Boolean functions
F1(A,B,C) = ∑(0,1,2,4)
F2(A,B,C) = ∑(0,5,6,7) using
i) PLA ii) PAL iii) ROM (16)

15. (a) Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0, the output does not change for any change in X. Use SR latch for implementation of the circuit. (16)

Or

(b) Design a clocked sequential circuit with single input *X* and single output *Z*. The circuit produces an output *Z*=1 whenever the input *X* completes the sequence 10111 and overlapping is allowed. Obtain the state transition table and implement using D flip-flops. (16)