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Question Paper Code: 39403

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2018

Elective

Electronics and Communication Engineering

01UEC903 - COMPUTER ARCHITECTURE AND ORGANIZATION

(Regulation 2013)

Duration: Three hours

Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. Discuss the stored program concept.
2. Differentiate direct and indirect addressing mode.
3. Compare spatial expansion and temporal expansion.
4. Discuss the principle behind the Booth's multiplier.
5. What is microprogramming?
6. What is Write-After-Write (WAW) hazard?
7. Define Hit ratio.
8. Define memory latency.
9. List out the limitations of the programmed I/O data transfer method.
10. What is memory mapped I/O?

PART - B (5 x 16 = 80 Marks)

11. (a) Briefly explain the organization of CPU and memory of the IAS computer with instruction set. (16)

Or

- (b) Explain the operation of each functional unit in the computer system with suitable diagram. (16)

12. (a) With a neat block diagram explain in detail about CPU-coprocessor interfacing. (16)

Or

- (b) With a neat sketch, explain in detail about logic design for fast adders. (16)

13. (a) Explain with a diagram the organization of a CPU incorporating a four stage instruction pipeline. (16)

Or

- (b) Explain the super scalar operations with a neat diagram. (16)

14. (a) Give the structures of semiconductor RAM memories. (16)

Or

- (b) Explain the concepts of memory hierarchies. (16)

15. (a) List out the three bus arbitration schemes. Explain any two with a diagram. (16)

Or

- (b) Explain in detail about standard I/O interfaces. (16)
