Reg. No. : | | | | | | | | | | |

Question Paper Code: 33506

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2018

Third Semester

Electronics and Instrumentation Engineering

01UEI306 – DIGITAL ELECTRONICS

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. What is 8421 code?
2. State De-Morgan's theorem.
3. Draw the schematic of three input TTL NAND gate.
4. Suggest a solution to overcome the limitation on the speed of the adder.
5. Compute the excitation table of T flip flop.
6. Differentiate between edge triggering and level triggering.
7. Differentiate fundamental mode and pulse mode asynchronous sequential circuits.
8. What is race conditions?
9. Discriminate between PLA and PAL.
10. Compare EPROM with EEPROM.

PART - B (5 x 16 = 80 Marks)

11. (a) Compute the minimized Boolean expression using K-map
F = A'BC'D'+A'BC'D+ ABC'D'+ AB'C'D+ A'B'CD' (16)

Or

(b) Given Y (A, B, C, D) = ∏M (0, 1, 3, 5, 6, 7, 10, 14, 15), draw the K-map and obtain the simplified expression and realize using basic gates (16)

12. (a) Design a full adder circuit and implement with the decoder circuit. (16)

Or

(b) Design a BCD to Excess-3 converter using truth table and k-map simplification. (16)

13. (a) Design a mod-7 synchronous binary counter using JK flip-flops. (16)

Or

(b) Design a 3-bit synchronous counter which counts in the sequence 000, 001, 011, 010,100, 110, (repeat) 000 using D flip flop. (16)

14. (a) Design a asynchronous sequential circuit specified by the following flow table. (16)

	00	01	10	10
A	A.O	A.O	A.O	B.0
B	A,O	A.O	B.1	B.1

Or

(b) Write short notes on races and hazards that occur in asynchronous circuits. (16)

15. (a) Implement the BCD to XS3 code conversion using ROM. (16)

Or

(b) Discuss about static and dynamic RAM cell. (16)

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