Reg. No.:					

(b) Three phase clock

(d) Four phase clock

## **Question Paper Code: 47504**

## B.E. / B.Tech. DEGREE EXAMINATION, MAY 2018

## Seventh Semester

## Electronics and Instrumentation Engineering

	14UEI/04 - VL	SI SYSTEM DESIGN	
	(Regul	ation 2014)	
ration: Three hours			Maximum: 100 Marks
	Answer A	ALL Questions	
	PART A - (10	$0 \times 1 = 10 \text{ Marks}$	
The limitations of scaling	g are		
(a) Broad channel effe	ects (b) na	arrow channel effects	
(c) interference effect	es (d) no	one of the above	
Source and drain in nMC	OS device are iso	olated by	
(a) A single diode (	b) Two diodes	(c) Three diodes	(d) Four diodes
If n-transistor conducts a	nd has large vo	ltage between source a	nd drain, then it is said to
be in region			
(a) Linear (b	o) Saturation	(c) Non saturation	(d) Non saturation
In basic inverter circuit,	is conne	ected to ground	
(a) Source (b)	o) Gates (	(c) Drain	(d) Resistance
In dynamic CMOS logic	is used		
	The limitations of scaling  (a) Broad channel eff  (c) interference effect  Source and drain in nMC  (a) A single diode (  If n-transistor conducts a  be in region  (a) Linear (li  In basic inverter circuit,  (a) Source (li	(Regularation: Three hours  Answer A  PART A - (1)  The limitations of scaling are  (a) Broad channel effects (b) na  (c) interference effects (d) no  Source and drain in nMOS device are is  (a) A single diode (b) Two diodes  If n-transistor conducts and has large vo  be in region  (a) Linear (b) Saturation  In basic inverter circuit, is connected.	Answer ALL Questions  PART A - (10 x 1 = 10 Marks)  The limitations of scaling are  (a) Broad channel effects (b) narrow channel effects  (c) interference effects (d) none of the above  Source and drain in nMOS device are isolated by  (a) A single diode (b) Two diodes (c) Three diodes  If n-transistor conducts and has large voltage between source a be in region  (a) Linear (b) Saturation (c) Non saturation  In basic inverter circuit, is connected to ground  (a) Source (b) Gates (c) Drain

(a) Two phase clock

(c) One phase clock

6.	Which multiplier is vo	ery well suited for	twos complement i	numebers?			
	(a) Baugh-wooley a	lgorithm (b	o) Wallace trees				
	(c) Dadda multipliers		(d) Modified booth encoding				
7.	Which type of PLD sh	ould be used to pr	ogram basic logic f	unctions?			
	(a) PLA	(b) PAL	(c) CPLD	(d) SLD			
8.	Which type of device	FPGA are?					
	(a) SLD	(b) SROM	(c) EPROM	(d) PLD bac	ck		
9.	What do VHDL stand f	or?					
	(a) Verilog hardwar	e description lang	uage (b) VHSIC ha	ardware description lan	guage		
	(c) very hardware d	escription languag	ge (d) VMEbus of	description language			
10.	In VHDL, which class operation?	of scalar data typ	e represents the value	ues necessary for a spec	cific		
	(a) Integer types	(b) Real types	(c) Physical type	(d) Enumerated	types		
		PART - B (5	$5 \times 2 = 10 \text{ Marks}$				
11.	What is depletion mod	le operation MOS	?				
12.	What is stick diagram	? What are the use	s of stick diagram?				
13.	What is a multiplier ci	rcuit?					
14.	What is programmable	e logic array?					
15.	What is LUT						
		PART - C (5	x 16 = 80 Marks)				
16.	(a) Explain in detail a mode and depletion		tor with the working	•	ment 6)		
	(b) Explain in detail a	bout the scaling co	Or oncept of MOS Trai	nsistor	(16)		
17.	(a) Explain about DC	Characteristics of	CMOS inverter circ	uit with neat diagram.	(16)		

Or	
(b) Explain in detail about the Stick Diagram and layout diagram.	(16)
18.(a) Discuss in detail about the Dynamic CMOS design.	(16)
Or	
(b) Explain multiplication with an example and discuss the types of multipliers.	(16)
19. (a) Explain in detail about FPGA Interconnecting Procedure.  Or	(16)
(b) Explain in detail about Floor planning, Routing &Placement.	(16)
20. (a) Write VHDL testbench code for 4:1 multiplexer.	(16)
Or	
(b) Write VHDL program for Half adder & Full adder.	(16)