Reg. No. : | | | | | | | | | | |

Question Paper Code: 37504

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2018

Seventh Semester

Electronics and Instrumentation Engineering

01UEI704 - VLSI SYSTEM DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. What are the second order effects in a MOS transistor?
2. What are the advantages of Twin-tub process?
3. Define short channel devices.
4. Indicate the different symbols used for various regions in stick diagram.
5. What are the advantages of AOI implementation of two level logic functions?
6. List the few applications of Tally circuits.
7. What are the advantages of PLA?
8. Mention some of PLDs.
9. List out the operators in VHDL.
10. What are the different design units in VHDL?

PART - B (5 x 16 = 80 Marks)

11. (a) (i) Show the various components of nMOS transistor model. (6)

(ii) Elaborate the process and steps involved in CMOS Fabrication of VLSI system technology. (10)

Or

(b) Explain the operation of MOS transistor in depletion mode and enhancement mode. (16)

12. (a) Draw the CMOS inverter transfer characteristics and explain its operation, clearly indicating the various regions. (16)

Or

(b) Determine the pull-up to pull down ratio for an nMOS inverter driven by another nMOS inverter. (16)

13. (a) Explain with neat diagrams the design of 4:1 multiplexer using dynamic CMOS and Domino logic. (16)

Or

(b) Explain the design and working of carry look ahead adder. (16)

14. (a) Explain the general architecture of FPGA and bring about different programmable blocks used. (16)

Or

(b) Explain in detail about planning placement and routing techniques of FPGA. (16)

15. (a) Write a VHDL code to realize the 4-bit synchronous counter using structural modeling. (16)

Or

(b) Write the VHDL code for Finite State Machine using behavioral and structural modeling. (16)
