Reg. No. : | | | | | | | | | | |

Question Paper Code: 43023

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2017

Third Semester

Computer Science and Engineering

14UCS303 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

(Smith chart may be permitted)

PART A - (10 x 1 = 10 Marks)

1. The time between the start and completion of a task is referred to as

(a) Response time (b) Execution time (c) Throughput (d) Both a and b

2. The BSA instruction is

(a) Branch and Store Accumulator (b) Branch and Save return Address
(c) Branch and Shift Address (d) Branch and Show Accumulator

3. How many full adders are required for *k* bit addition?

(a) *k* (b) *k*+1 (c) 2*k* (d) *k*-1

4. The processor keeps track of the results of its operations using a flags called

(a) Conditional code flags (b) Test output flags
(c) Type flags (d) None of these

5. The condition observed in the following sequence of instructions is

Add *r*1,*r*2
Add *r*1,*r*3

(a) Data hazard (b) Data dependence
(c) Structural hazard (d) Normal sequence

6. The throughput of an ideal pipeline with *k* stages is _____ instruction/clock cycle.

(a) *k* (b) *k*-1 (c) 1 (d) 2

7. The cost of parallel processing is primarily determined by

(a) Time complexity (b) Switching complexity
(c) Circuit complexity (d) None of the above

8. When instruction i and instruction j are tends to write same register or memory location, it is called

(a) Input dependence (b) Output dependence
(c) Ideal pipeline (d) Digital call

9. The signal sent to the device from the processor to the device after receiving an Interrupt is

(a) Interrupt-acknowledge (b) Return signal
(c) Service signal (d) Permission signal

10. The extra time needed to bring the data into memory in case of a miss is called as

(a) Delay (b) Propagation time (c) Miss penalty (d) Data latency

PART - B (5 x 2 = 10 Marks)

11. Why the data bus is bidirectional while the address bus is unidirectional?

12. What is the purpose of guard bits in floating point operations?

13. How do you handle the data hazard?

14. Define interleaved or fine grained multithreading.

15. What is polling?

PART - C (5 x 16 = 80 Marks)

16. (a) What do you mean by addressing modes? Explain the types of addressing modes that exists in modern processors? (16)

Or

(b) (i) Describe the different classes of Instruction format with examples. (12)

(ii) Registers *R*1 and *R*2 of a computer contain the decimal values 1200 and 2400 respectively. What is the effective address of the memory operand in each of the following instructions?

Load 20(*R*1), *R*5

Add –(*R*2), *R*5 (4)

17.(a) (i) Illustrate non-restoring division algorithm with an example. (8)

(ii) Design a 16-bit carry- look ahead adder using 4-bit adders and explain. (8)

Or

(b) Derive and explain an algorithm for adding and subtracting two floating point binary numbers. (16)

18. (a) Explain the super scalar operations with a neat diagram. (16)

Or

(b) State and explain the different types of hazards that can occur in a pipeline. (16)

19. (a) Explain Flynn's classification of computers. (16)

Or

(b) Discuss in detail instruction level parallelism. (16)

20. (a) Explain the virtual memory address translation and TLB with necessary diagram. (16)

Or

(b) What is virtual memory? Explain the address translation scheme. (16)

43023