Reg. No. : | | | | | | | | | | |

Question Paper Code: 33203

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2018

Third Semester

Computer Science and Engineering

01UCS303 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. Define big Endean and little Endean format.
2. What do you mean by stored program concept?
3. What is Subword Parallelism?
4. List the features of booth multiplication algorithm
5. What is control hazard?
6. Define branch folding.
7. Give an example for WAW Hazard.
8. What is instruction level parallelism?
9. What is Rotation Latency?
10. Define Bus. What are the different buses in a CPU?

PART - B (5 x 16 = 80 Marks)

11. (a) (i) Explain the components of computer system. (8)

    (ii) Explain in detail the different types of instructions that are supported in a typical processor. (8)

Or

(b) Write in detail about various addressing modes. (16)

12. (a) Explain the MIPS Multiplication and Division process with hardware architectural diagram. (16)

Or

(b) Explain the floating point addition steps and algorithm in detail. (16)

13. (a) Explain the complete datapath functions of the multicycle implementation with architectural diagram. (16)

Or

(b) Discuss the various hazards that might arise in a pipeline. What are the remedies commonly adopted to overcome/minimize these hazards. (16)

14. (a) Explain the Multiple-instruction multiple-data streams (MIMD) parallel architecture functions with suitable block diagram. (16)

Or

(b) Discuss in detail about Flynn's classification. (16)

15. (a) Explain the different ways used for improving the cache performance. (16)

Or

(b) How does a virtual address get translated into physical address? Explain in detail with the neat diagram. Explain the use of TLB. (16)