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Reg. No. : | | | | | | | | | | |

Question Paper Code: 52208

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2018

Second Semester

Computer science and Engineering

15UCS208 - DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. The binary equivalent of (1011.011)10 is equal to CO1- R

(a)11.375 (b) 10.123 (c) 11.175 (d) 9.234

2. What is the major difference between half-adders and full-adders? CO2- R

(a) Full-adders are made up of two half-adders

(b) Full adders can handle double-digit numbers

(c) Full adders have a carry input capability

(d) Half adders can handle only single-digit numbers

3. The inputs in the PLD is given through CO3- R

(a) NAND gates (b) OR gates (c) NOR gates (d) AND gates

4. The sequential circuit is also called CO4- R

(a) Flip-flop (b) Latch (c) Strobe (d) None of the Mentioned

5. In asynchronous circuit, changes occur with change of CO5- R

(a) input (b) output (c) clock pulse (d) time

PART – B (5 x 2= 10Marks)

6. List the number systems CO1- R
7. What is code conversion? CO2- R
8. List basic types of programmable logic devices CO3- R
9. What is the difference between synchronous and asynchronous counter? CO4- R
10. List out the steps for the design of asynchronous sequential circuit CO5- R

PART – C (5 x 16= 80Marks)

11. (a) (i) Explain BCD Code with Examples CO1-U (8)

(ii) List out the Procedure for converting Binary to Gray Code and give the example. CO1-U (8)

Or

(b) (i) State and prove DeMorgan's theorem CO1-U (8)

(ii) Simplify the following function into sum-of-products form and product of sums form(using K-Map) $F(A,B,C,D) = \Sigma(0,1,2,5, 8, 9, 10)$ CO1-U (8)

12. (a) (i) Explain the Design procedure for Combination Logic Circuits. CO2-U (8)

(ii) Explain the Logic implementation of half–adder and half-subtractor. CO2-U (8)

Or

(b) (i) Explain Logical Implementation of Full – adder and Full – Subtractor. CO2-U (8)

(ii) Draw the Logic Diagram for BCD to Excess 3 code Converter and Explain. CO2-U (8)

13. (a) (i) Design the 4 to 1 line Multiplexer and analyze its functionalities CO3- App (8)

(ii) Design the Logic Diagram of 3 to 8 line Decoder and analyze its functionalities. CO3- App (8)

Or

	(b)	(i) Define Memory and discuss the operation & types of RAM and ROM.	CO3-U	(8)
		(ii) Explain the Programmable Logic array.	CO3-U	(8)
14.	(a)	(i) Describe S-R Flip Flop with neat diagram	CO4- U	(8)
		(ii) Describe D Flip Flop with neat diagram	CO4- U	(8)
		Or		
	(b)	(i) Explain Serial in Serial out Shift Register with neat diagram.	CO4- U	(8)
		(ii) Draw a 3 bit binary Up-Down counter and explain it.	CO4- U	(8)
15.	(a)	With suitable example and diagram explain the hazards in combinational and sequential logic circuits.	CO5- U	(16)
		Or		
	(b)	With necessary example and diagram explain the concept of reduction of state and flow tables.	CO5- U	(16)

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