Reg. No. : | | | | | | | | | | |

Question Paper Code: 42207

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2018

Second Semester

Computer Science and Engineering

14UCS207 – DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 1 = 10 Marks)

1. The output of an AND gate is LOW _____.
   (a) when any input is LOW (b) when any input is HIGH
   (c) when all inputs are HIGH (d) all the time
2. When used with an IC, what does the term "QUAD" indicate?
   (a) 4 circuits (b) 2 circuits (c) 8 circuits (d) 6 circuits
3. Which of the following expressions is in the sum-of-products (SOP) form?
   (a) AB + CD (b) AB(CD) (c) (A + B)(C + D) (d) (A)B(CD)
4. The systematic reduction of logic circuits is accomplished by:
   (a) symbolic reduction (b) using Boolean algebra
   (c) TTL logic (d) using a truth table
5. Boolean algebra is also known as
   (a) Gate algebra (b) Transistor algebra (c) Switching algebra (d) Counting algebra
6. 3 bits full adder contains
   (a) 3 combinational inputs (b) 4 combinational inputs
   (c) 6 combinational inputs (d) 8 combinational inputs

7. HDL stands for

(a) Hardware Description Language (b) Hardware Design Language
(c) High Design Language (d) High Description Language

8. Flip flop is to

(a)Store octal value (b) Store hexadecimal value
(c) Binary value (d) ACCII value

9. Combinations that are not listed for input variables are

(a) overflows (b) carry (c) dont cares (d) zero bits

10. _____unwanted switching transients that may appear at the output of a circuit is known as

(a) Hazards (b) Cycles (c) Races (d) Critical Race

PART - B (5 x 2 = 10 Marks)

11. Show that the dual of the exclusive-OR is equal to its complement
12. Explain the design procedure for combinational circuits.
13. Give the applications of Demultiplexer.
14. Define race around condition.
15. What is a state equation?

PART - C (5 x 16 = 80 Marks)

16. (a) Reduce the following expression to the SOP and POS form

$$Y(W, X, Y, Z) = \sum m(1, 2, 3, 5, 9, 12, 14, 15) + \sum d(4, 8, 11).$$ (16)

Or

(b) How would you express the Boolean function using K-map and draw the logic diagram

$F(w,x,y,z) = \sum m(0,1,2,4,5,6,8,9,12,13,14)$ (16)

17. (a) Explain in detail a binary multiplier. (16)

Or

((b) Demonstrate 4-bit magnitude comparator with three outputs: A>B, A=B and A<B. (16)

18. (a) (i) Implement the following Boolean function with a 4:1 multiplexer and external gates.

$F(A, B, C, D)=\sum(1, 3, 4, 11, 12, 13, 14, 15)$. (8)

(ii) Using a decoder and external gates, design the combinational circuits defined by the following three Boolean functions:

$F1=x'y'z' +xz +yz$

$F2=xy'z' + x'y$

$F3=x'y'z + xy$ (16)

Or

(b) (i) How would you design a 3:8 decoder using basic gates? (8)

(ii) Deduce the design of a 1:4 Demultiplexer circuit. (8)

19. (a) (i) Construct and explain the working of a 4-bit Up/Down ripple counter. (8)

(ii) Model a synchronous MOD-5 counter and explain with waveforms. (8)

Or

(b) A sequential circuit has two flip flops (A and B), two inputs (x and y) and an output (Z). The flip flop input functions and the circuit output function are as follows.

JA = XB + y'B KA = xy'B'

JB = xA' KB = xy' + A

Z = xyA + x'y'B

Obtain the logic diagram; sate table, state diagram and state equations. (16)

20. (a) (i) What is a Hazard? Give hazard free realization for the following Boolean function. $F(A, B, C, D) = \Sigma m(0, 2, 6, 7, 8, 10, 12)$. (8)

(ii) Find the ASM chart for binary multiplier. (8)

Or

(b) Write short notes with an example for

(1) Shared row state assignment

(2) One hot state assignment (16)