Reg. No. : | | | | | | | | | | |

Question Paper Code: 32207

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2018

Second Semester

Computer Science and Engineering

01UCS207- DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Convert $(101101.1101)_2$ to decimal and hexadecimal form?
2. What is a logic gate??
3. Write down the truth table of a full subtractor.
4. Develop a HDL program module for half-adder.
5. Name the different HDLs.
6. Compare SRAM and DRAM.
7. Give the classification of PLDs.
8. What is a primitive flow table?
9. Define race condition.
10. List the assumptions that must be made for a fundamental mode circuit.

PART - B (5 x 16 = 80 Marks)

11. (a) Reduce the following function using K-map technique and implement the reduced Boolean expression with basic gates

$f(A, B, C, D) = \pi M (0, 3, 4, 7, 8, 10, 12, 14) + d (2, 6)$. (16)

Or

(b) Minimize the expression using Quine McCluskey method (Tabulation) method $F=\sum m(0, 1,9, 15, 24, 29, 30)+\sum d(8, 11, 31)$. (16)

12. (a) Design a circuit that converts 8421 BCD code to Excess 3 code. (16)

Or

(b) (i) Design a full adder circuit with necessary diagram. (10)

(ii) Write the HDL description of the circuit specified by the following Boolean function. (6)

13. (a) Implement the following Boolean function using a 8 to 1 multiplexer F(A, B, C, D) = A'BD'+ ACD+ B'CD+ A'C'D. Also implement the function using 16 to 1 multiplexer. (16)

Or

(b) Implement the Boolean function using 8:1 multiplexer

$F(A, B, C, D) = AB' D + A' C' D + B' CD' + AC' D$. (16)

14. (a) Design a 4-bit binary ripple counter using D flip-flops. (16)

Or

(b) (i) Explain in detail about parallel in serial out shift register, with neat sketches. (10)

(ii) Write the HDL for full adder circuits. (6)

15. (i) Describe the design procedure for asynchronous sequential circuits. (10)

(ii) Write short notes on ASM chart. (6)

Or

(b) Implement the Switching Function F=∑m(1, 3, 5, 7, 8, 9, 14, 15) by a static hazard free two level AND OR gate network. (16)