Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 60686

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Fourth Semester

Instrumentation and Control Engineering

IC 2251/IC 43/EC 1263 A/10133 IC 403/080260004 — DIGITAL PRINCIPLES AND DESIGN

(Regulations 2008/2010)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Design a half adder using logic gates.

2. Realize the function $F = \Sigma m(0, 1, 3, 6, 7)$ using 8 : 1 multiplexer.

3. Show how a JK flip-flop can be operated as a T flip-flop? Apply a 10 KHz square wave as input and determine the output frequency.

4. What is meant by a shift register? List any two types.

5. Implement two input XOR gate using 2 to 1 multiplexer.

6. List out the special features for Field Programmable Gate array devices.

7. What are the merits and demerits of the TTL family?

8. List the characteristics of ECL logic gates.

9. List the characteristics of CMOS family.

10. Why does the MOS family mostly use NMOS devices?

PART B — (5 × 16 = 80 marks)

11. (a) Use Quine McCluskey method to find a minimum cost SOP realization of the function $f(x1, x2, x3, x4) = \Sigma m\,(2, 3, 5, 6, 7, 10, 11, 13, 14)$. (16)

Or

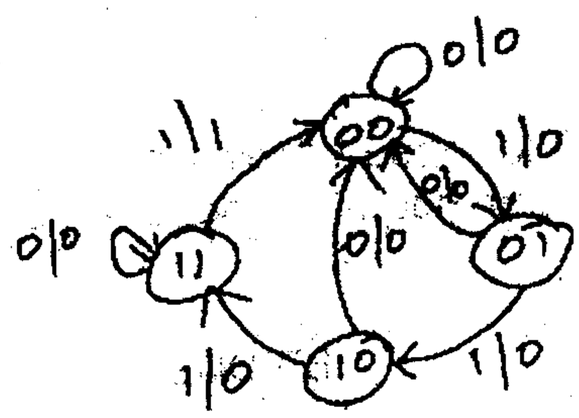
(b) (i) Show how the function $f(w1; w2, w3) = \Sigma m(0, 2, 3, 4, 5, 7)$ can be implemented using 3 to 8 binary encoder and OR gate. (8)

(ii) Explain the operation of Full-Adder circuit with truth table and circuit diagram. (8)

12. (a) Design a 4 bit up/down synchronous counter using JK flipflops and explain its operation. (16)

Or

(b) For the given state diagram design a sequential circuit using D flipflops.



13. (a) (i) Implement the following Boolean expressions using ROM :

$F_1(A,B,C) = \Sigma m(0, 1, 3, 5)$

$F_2(A,B,C) = \Sigma m(0, 3, 5, 7)$ (9)

(ii) Realize the following function using 8 : 1 MUX

$F(A,B,C) = \Sigma m(0, 2, 4, 6, 7)$. (7)

Or

(b) (i) Tabulate the PLA programmable table for the four Boolean functions listed below and minimize the number of product terms :

$F_1 = (x, y, z) = \Sigma m(1, 2, 4, 6)$

$F_2 = (x, y, z) = \Sigma m(0, 1, 6, 7)$

$F_3 = (x, y, z) = \Sigma m(2, 6)$

$F_4 = (x, y, z) = \Sigma m(1, 2, 3, 5, 7)$. (12)

(ii) Write short note on CPLD. (4)

14. (a) Draw and explain the interface of the following :

(i) TTL driving CMOS load (8)

(ii) CMOS driving TTL load. (8)

Or

(b) (i) List and explain the characteristics of MOS logic families. (8)

(ii) Mention the advantages of ECL over other IC technologies. (8)

15. (a) (i) Derive a CMOS complex gate for the logic function $F = AB + AC + BC$. (10)

(ii) Explain why are MOS ICs especially sensitive to static charge? (6)

Or

(b) (i) Explain the important characteristics of NMOS logic. (6)

(ii) Draw and explain the basic NMOS NAND and NOR gates. (10)
