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Question Paper Code : 60505

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Fourth Semester

Electrical and Electronics Engineering

EE 2255/EC 1261 A/EE 46/ 080280029/10133 EE 406 A – DIGITAL LOGIC CIRCUITS

(Common to Electronics and Instrumentation Engineering)

(Regulations 2008/2010)

(Also common to PTEE 2255 – Digital Logic Circuits for B.E. (Part-Time) Third Semester – EEE – Regulations 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw OR gate using NAND gates.

2. Give any two applications of decoders.

3. What is the drawback of RS flip flop?

4. What is state reduction?

5. What are the drawbacks of asynchronous sequential circuits?

6. What are race conditions?

7. Which digital logic family would you choose if
   (a) Faster operation is required
   (b) Low power consumption is required.

8. What are the techniques adopted for erasing E PROM?

9. What are the advantages of VHDL?

10. What are the objectives for choosing test benches?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Simplify :

(1) $AB'+A'B'D+A'CD'$

(2) $AB'+AB'CD+ABC'D'$. (4)

(ii) Convert the following expressions to product-of-sums form

(1) $WX'Y+WXZ'+Y'Z$

(2) $AB'C'+CD'+BC'D'$. (4)

(iii) Design 2 × 4 decoder and show how it can be converted into 1 × 4 demultiplexer. (8)

Or

(b) (i) Simplify the following expression using Karnaugh map and Quine McCluskey method. Compare the results. (8)

$A'BC'+BC'D'+A'CD+B'CD+A'BD$

(ii) Design an 8421 to excess-3 code converter. Draw the logic diagram. (8)

12. (a) (i) Convert a clocked D flip flop to a clocked JK flip flop using external gates. (4)

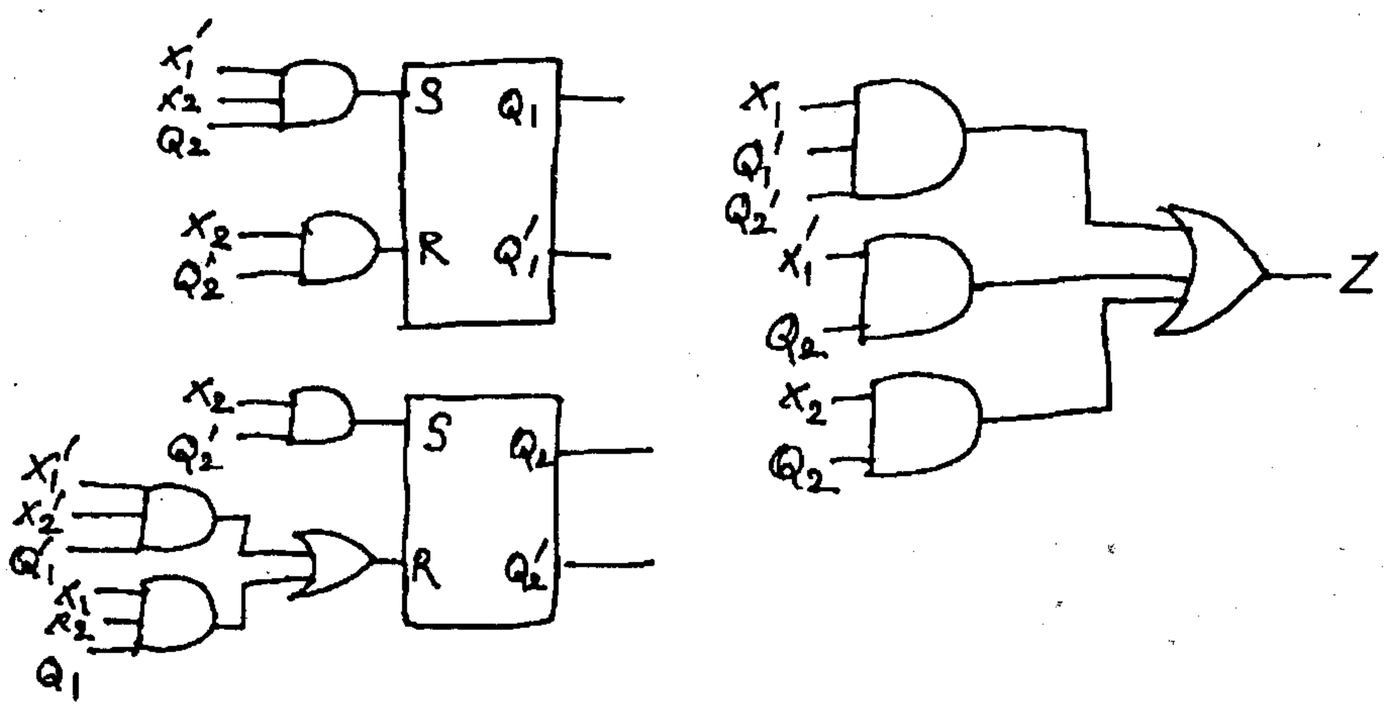
(ii) Design cyclic shift registers using JK flip flops. (12)

Or

(b) Design a counter which counts in the following sequence using D flip flops.

0000, 1000, 1100, 1010, 1110, 0001, 1001, 1101, 1011, 1111, 0000..... (16)

13. (a) For the following network, construct a flow table and determine the output sequence. The initial state is 00 and the input sequence is $X_1X_2 = 00, 01, 11, 10, 00$. (16)



Or

(b) Make a proper assignment of internal state variables for the following state transition table on flow table. Specify the final state tables interms of the internal states. (16)

	00	01	11	10
1	①	①	4	5
2	1	②	②	5
3	③	1	2	③
4	3	2	④	5
5	3	⑤	2	⑤

14. (a) (i) Give the PLA table to implement the following equations : (8)

$X = ABD + A'C' + BC + C'D'$

$Y = A'C' + AD + C'D'$

$Z = CD + A'C' + AD + AB'D$

(ii) Design a circuit using ROM for the above equations. (8)

Or

(b) (i) Draw the circuit of a four – input NAND gate using CMOS transistors. (8)

(ii) Write the characteristics of TTL and CMOS families. (8)

15. (a) (i) Explain the function of the circuit specified by the following HDL code.

```
Module prob (A, B, S, E Q) ;
input [1 : 0 ] A, B;
input S, E ;
output [1 : 0] Q ;
assign Q = E? (S ? A : B) : 'bZ ;
end module.
```

(8)

(ii) Write an HDL data flow description of a 4-bit adder subtractor of unsigned numbers. (8)

Or

(b) Write the HDL code for ripple counter. (16)
