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Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 60540

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Eighth Semester

Electrical and Electronics Engineering

EI 2403/EI 73/10144 EC 605 — VLSI DESIGN
(Common to Seventh Semester – Electronics and Instrumentation Engineering and Eighth Semester – Instrumentation and Control Engineering)

(Regulations 2008/2010)

(Also common to EI 2403/10144 EC 605 – VLSI Design for B.E. (Part-Time) Seventh Semester – EEE – Regulations 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the second order effects of the MOSFET device?

2. List the factors which affect the threshold voltage of a MOS transistor.

3. Draw a CMOS inverter.

4. Draw the stick diagram for an NMOS inverter.

5. Draw CMOS logic for XOR gate.

6. What is clock skew?

7. Write the two special classes of FPLA.

8. What are the factors that determine the overall size of a PLA?

9. Name the data types supported by VHDL.

10. Write the VHDL code for 4 by 1 Multiplexer.

PART B — (5 × 16 = 80 marks)

11. (a) Discuss in detail about the second order effects of MOS transistor with relevant expressions. (16)

Or

(b) Explain in detail with schematic, the basic CMOS fabrication process. (16)

12. (a) Design a digital BiCMOS circuit that implements the function $f = c.k.r + r.k.p$.

Or

(b) (i) Draw the stick diagram for a XOR gate. (6)

(ii) Discuss the transfer characteristics, output characteristics, Pull up – Pull down ratios, timing and fan-out consideration of a CMOS inverter. (10)

13. (a) (i) Describe the operation of an NMOS and a CMOS exclusive – OR structure. (8)

(ii) Explain the various methods to improve the speed of four bit adders. (8)

Or

(b) (i) Explain the operation of 4 × 4 NMOS barrel shifter with neat diagrams. (8)

(ii) Draw and explain the NMOS and CMOS implementation of a 4 to 1 MUX. (8)

14. (a) Explain the NMOS implementation of PLA and discuss the applications of PLA in finite state machines. (16)

Or

(b) Draw and explain the architecture of FPGA and discuss its applications. (16)

15. (a) (i) Write the format of PROCESS statement in VHDL. (6)

(ii) Write the VHDL code for 4 bit adder calling full adder as component. (10)

Or

(b) (i) Write short notes on need for Test benches. (6)

(ii) Write the VHDL code for 8 bit counter. (10)